Universidade de Aveiro Departamento de Electrónica, Telecomunicações e Informática

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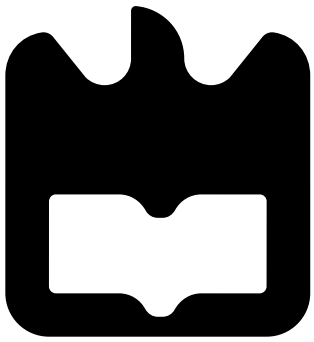
João Lucas Rodrigues Silva

Amplificador RF de Potência Outphasing-Chireix



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Dissertação apresentada à Universidade de Aveiro para cumprimento dos requisitos necessários à obtenção do grau de Mestre em Engenharia Eletrónica e Telecomunicações, realizada sob a orientação científica do Dr. José Carlos Pedro, Professor catedrático e do Dr. Pedro Miguel Cabral, Professor auxiliar, ambos do Departamento de Eletrónica Telecomunicações e Informática da Universidade de Aveiro.

Dedico este trabalho à minha família, amigos e em especial à minha namorada, que sempre mostrou o seu apoio ao longo deste percurso.

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Agradecimentos

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Palavras-Chave Amplificador de Potência,de Rádio Frequência, Combinador Chireix, Estação Base, Load Pull, Outphasing.

Resumo Esta dissertação tem como objetivo estudar e implementar um amplificador de potência de Rádio Frequência utilizando o conceito de Outphasing, proposto por H. Chireix em 1935, mas que nos recentes anos tem vindo a ser objeto de estudo intensivo, não só ao nível académico, mas também pelos grandes fabricantes de amplificadores de potência de Rádio Frequência. Assim, este trabalho foi desenvolvido com o objetivo de seguir as tendências de mercado e detetar os principais problemas relacionados com a sua implementação, para mais tarde, ser capaz de apresentar algo de relevante ao mercado e de acordo com as suas necessidades. Deste modo, implementou-se um sistema Outphasing com um Combinador Chireix a uma frequência de 1.8 GHz, apresentando uma eficiência máxima de 60% e uma eficiência de 40% a 10dB da potência máxima quando em operação em onda contínua. Este amplificador de potência foi projetado com dois amplificadores diferentes a operar em class E, combinando o conceito de Outphasing com modulação em amplitude, com vista a melhorar a sua eficiência total e linearidade.

Keywords Base Station, Chireix Combiner, Load Pull, Outphasing, Radio Frequency Power Amplifier.

Abstract The objective of this dissertation is to study and implement a RF Power Amplifier using the Outphasing concept, which was proposed by H. Chireix in 1935 but, in the recent years, has been the subject of intensive research, not only at the academic level, but also by the big manufacturers of Radio Frequency Power Amplifiers. Thus, this work was developed to follow market tendencies and detect the most significant problems related with its implementation to, later on, be capable to present something interesting to the market, according to its requirements. So, an Outphasing Amplifier using a Chireix Combiner for 1.8 GHz was implemented, presenting a peak Power added efficiency of around 60% and almost 40% at 10 dB of Output power back off in Continuous wave. This Power Amplifier was designed with two different class E amplifiers, mixing also the concept of Outphasing with Amplitude modulation, in order to increase its efficiency and to linearize it at the same time.

Contents

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Acronyms

ADS	Advanced Design System
AC	Alternate Current
AM	Amplitude Modulation
CW	Continuous Wave
DC	Direct Current
LINC	Linear Amplification with non Linear Components
OPBO	Output power back-off
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak-to-Average Power Ratio
PDF	Probability Density Function
PM	Phase Modulation
PF	Power Factor
RF	Radio Frequency
VSG	Voltage Signal Generator

1. Introduction

Due to the continuous demand for higher data rates in telecommunication systems, various techniques of signal modulation have been proposed. However, it seems inevitable to rely on signals of variable envelope, where it remains a hard task having Power Amplifiers (PA) operating with high efficiency. The problem is very simple: to obtain different powers at the PA output, it is either needed to excite the PA with different powers at the input, to modulate the supplied power or to vary the load. The first solution compromises the efficiency, since the majority of PAs used are linear and their efficiency is proportional to the input signal. The second solution requires highly efficient and high-speed power supply modulators yet to be designed. The third solution is wiser but also more complex. The idea is to change the load dynamically, obtaining different power signals at the output and keeping the input signal constant. In this field, the Doherty Amplifier [1] seems to be, by far, the best solution, yet, it is limited by the efficiency of the class B Amplifier [2].

In 1935, H. Chireix proposed the Outphasing model, enabling the use of highly efficient PAs architectures. This model is known as LINC (Linear amplification with Nonlinear Components) system, which operates always with the transistors highly saturated. By changing their phase, it is possible to modulate the input signal and then recover it through a combiner.

At first glance, one might think that the main reason for using highly efficient amplifiers is to go beyond the efficiency of the class B. Yet, as it will be explained in Chapter 2, the load seen by each PA depends on the phase difference between the input signals and therefore, the waveforms presented on the drain will also change according to the load variation, having a direct impact on the PA efficiency. However, if the transistor operates in a highly saturated mode, a small load variation, despite changing the output power, will not be significant to the PA efficiency, as it will be demonstrated in Chapter 3.

This load variation has proved to be symmetrical, being more inductive for one PA and capacitive for the other. So, and in order to improve the efficiency at a considerable Output Power Back-OFF (OPBO), H. Chireix proposed to compensate these reactances with a capacitance and an inductance before the combiner.

The objective of this dissertation is to study and design an Outphasing system proving its concept, making it as linear as possible. Thus, in Chapter 4, besides describing the steps that had to be followed to design a highly efficient Outphasing arrangement, it is also explained how this system can be linearized, keeping its efficiency as high as possible. As a way to show more capabilities of this system, three techniques were added to this work.

The first one is motivated by the fact that, for lower output powers, the system becomes very inefficient. So, to overcome this handicap, the input power of both PAs was reduced, making them operating as class B PAs.

Afterwards, it was concluded that this system could be more efficient if the output matching networks of each PA were adapted for the impedance presented to them, separately. Lastly, the amplitude and phase of the input signal of each PA were handled simultaneously, increasing the Power Added Efficiency (PAE).

In the last chapter, the designed system is presented and its results discussed. Despite the fact that they are a little different from their corresponding simulations, good results were obtained for a first prototype.

2. Outphasing Concept

Before designing or implementing a Chireix amplifier, the Outphasing concept has to be fully understood. So, this chapter starts to explain how an amplitude signal can be represented by two signals with a certain phase, being recovered then with an analog combiner. After that, a mathematical analysis is done to predict the impedance that will be presented at each PA. Although it is represented only the equations deduced, their deductions can be consulted in the Appendix B. In the end, those results will be validated through the Advanced Design System (ADS) simulator, using a nonlinear model to represent each transistor.

2.1 AM-PM Modulator

Let us consider a Continuous Wave (CW) signal, represented as $Acos(wt)$, in which A is the Amplitude and ω is the angular frequency. Let us assume also that this CW signal can be represented as the sum of two CW signals, with equal amplitude K and modulated with symmetric phase, θ, eq. 2.1. By expressing this equation with respect to θ, eq. 2.2, the equation becomes solvable and determined for certain values of A, meaning that a replica of the input signal can be recovered from $S_1(t)$ and $S_2(t)$ signals, fig. 2.1.

$$S_1(t) = Kcos(wt + \theta)$$
$$S_1(t) = Kcos(wt - \theta)$$

$$Acos(wt) = Kcos(wt + \theta) + Kcos(wt - \theta) \quad (2.1)$$

$$\theta = \cos^{-1}\left(\frac{A}{2K}\right) \quad (2.2)$$

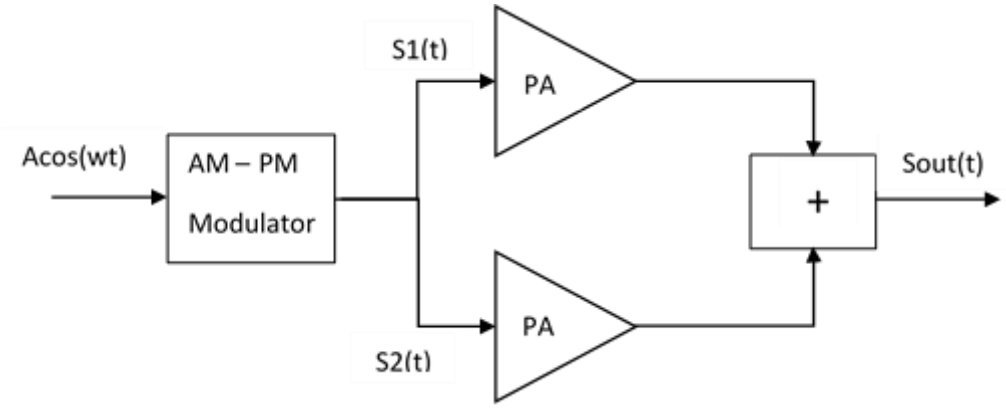

Figure 2.1 – Block diagram of an Outphasing Amplifier

Despite being possible to recover the input signal, there are some limitations to the maximum amplitude that can be represented. Since eq. 2.2 imposes that $\frac{A}{2K}$ cannot be greater than 1, A is limited to the double of K and so the output cannot be greater than two times the amplitude of the PAs. As the phase of the original signal is preserved, signals modulated in amplitude and phase can be used in this topology.

2.2. Outphasing Amplifier

2.2.1. Differential Circuit

After the signals have been amplified, they must be added. So, H. Chireix proposed a model in which two voltage signals, V_1 and V_2, are delivered to a resistor in opposite terminals, resulting on a current whose amplitude is dependent on the phase difference between these two signals, fig. 2.2.

Defining the source voltages by eq. 2.3 and 2.4, it can easily be concluded that the current that flows on the resistance can be expressed by eq. 2.5.

$$V_1 = Ke^{j\theta} \tag{2.3}$$

$$V_2 = Ke^{-j\theta} \tag{2.4}$$

$$Iout = \frac{V1-V2}{RL} = \frac{j*2K\sin(\theta)}{RL} \tag{2.5}$$

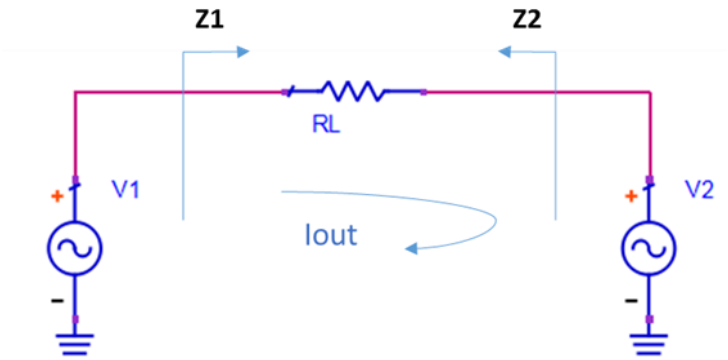

Figure 2.2 – Differential circuit representing Outphasing configuration

Since the current loop that includes the load also contains the sources, the current that crosses the load, I_{Load}, is the same that crosses the voltage sources. Therefore, the impedance seen by each source voltage will be directly dependent on the I_{Load}.
As the current varies with θ, the impedance seen by each source voltage must also vary. Otherwise, the power delivered to the load would always be the same, since there is no other dissipative element in the circuit than the resistor. This explanation demystifies the concept that in the Outphasing arrangement PAs are always delivering the same power into the same load, eq. 2.6 and 2.7.

$$Z_1 = \frac{V_1}{I_0} = \frac{1}{2} R_L (1 - j * cot(\theta)) \tag{2.6}$$

$$Z_2 = \frac{V_2}{I_0} = \frac{1}{2} R_L (1 + j * cot(\theta)) \tag{2.7}$$

Furthermore, it can be concluded that the maximum power is delivered for θ=90 and when θ=0, there is no current flowing on the circuit. Consequently, there is also no power on the load.

2.2.2. Practical Circuit

The circuit described previously does not have a common ground and so it cannot be used in monopole or patch antennas due to the fact that they are single-ended. Besides that, a transmission line is required to connect both amplifiers to the same output. Although a balanced-to-unbalanced transformer could be used, some works have proved that they present losses at GHz frequencies [26]. The next circuit, fig. 2.3, is an alternative way to circumvent these obstacles. However, the impedance seen by each amplifier has a different behaviour, as well as the current to the load, eq. 2.8, 2.9 and 2.10. This load modulation seen by each source could be solved if a resistor was used between each source voltage as in the Wilkinson Combiner. However, and despite the load seen by each source would be the same, the power that would not be delivered to the load would be dissipated on this resistor.

$$Z_1{}' = \frac{V_1}{I_1} = \frac{1}{2}\frac{{Z_0}^2}{R_L}[1 + jtan(\theta)] \tag{2.8}$$

$$Z_2{}' = \frac{V_2}{I_2} = \frac{1}{2}\frac{{Z_0}^2}{R_L}[1 - jtan(\theta)] \tag{2.9}$$

$$I_{Load} = \frac{-j2Kcos(\theta)}{Z_0} \tag{2.10}$$

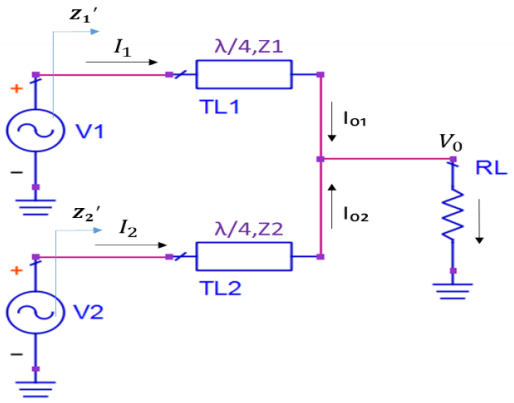

Figure 2.3 – Practical configuration using transmission lines

As indicated in eq. 2.10, the current on the load is now proportional to cos(θ). This arises due to the sum of the currents provided by the current sources.

Both topologies are considering a voltage source as a signal generator, since the Chireix Amplifier is done with saturated amplifiers. Yet, and in order to simplify the circuit, these

theoretical results will be tested with linear amplifiers, which is the same as having a current source as signal generator. Thereby, it is needed to do some changes in this circuit.

2.3. Simulation

2.3.1. Chireix Amplifier without compensation

Previously, it was said that the transmission line was added to convert the voltage source into a current source. Yet, since the PA that will be considered is operating in class B, the voltage source has to be substituted by a current source and so, the transmission line is no longer needed, at least for a while.
So, considering that now K is the amplitude of each current source, the current on the load will be the same as the one that was previously calculated, but without the influence of the transmission line, eq. 2.11. Therefore, different impedances are presented to each current source, eq. 2.12 and 2.13.

$$I_{Load} = 2Kcos(\theta) \tag{2.11}$$

$$Z_1 = 2 * R_L \left(cos(\theta)^2 - j\frac{sin(2\theta)}{2}\right) \tag{2.12}$$

$$Z_2 = 2 * R_L \left(cos(\theta)^2 + j\frac{sin(2\theta)}{2}\right) \tag{2.13}$$

Looking to these new impedances it can be seen that, not only the resistive impedance varies with θ but also that the absolute values are higher.
Assuming a VDD to bias the current source and an Imax as the maximum current at the output, assuming also that the current source is representing an ideal class B PA, the load that will guarantee the maximum power, the optimal load, R_{opt}, will be given by eq. 2.14, according to its loadline.

$$R_{opt} = \frac{2*VDD}{I_{max}} \approx 50\ \Omega \tag{2.14}$$

So, because of 2.12 and 2.13, the resistance seen by each current source is twice R_L. Then, R_L has to be half of the R_{opt} to ensure that the PA is operating at its maximum efficiency without saturation.

With the purpose to test the Chireix Combiner and to evaluate the expressions deduced, a simple circuit was designed in the ADS simulator. For that purpose, two current sources were placed together in parallel, followed by a resonator, converging then into a load through a combiner, fig. 2.6. Those current sources represent an ideal class B amplifier, wherein, their Direct Current (DC) curves are represented in figs. 2.4 and 2.5. Since they are being fed with 10V in their drain and in order to achieve their maximum efficiency, the output resistance of the system must be 25 ohms, as it was demonstrated in eq. 2.12 and 2.13.

Ideally, the efficiency of each PA would be given by the maximum efficiency of a class B PA. Nevertheless, the impedance presented to the PA is changing and so, as the power provided by each PA depends on the load presented to it, some authors use the Power Factor (PF), eq. 2.15, to define the efficiency of each PA. This is nothing more than the impact caused by the reactive impedance.

Notwithstanding, the real impedance presented to each PA is changing and so, as a direct consequence, the drain voltage also changes, increasing the power dissipated on each transistor, eq. 2.16.

Furthermore, the reactive impedance presented to each PA is also changing, decreasing the power delivered to the load, eq. 2.17.

$$PF = \frac{\sqrt{P_{active}{}^2}}{\sqrt{P_{active}{}^2 + P_{reactive}{}^2}} = cos(\theta) \quad (2.15)$$

$$\eta_{classB} = \frac{\pi}{4} * \cos(\theta) \quad (2.16)$$

$$\eta = \frac{\pi}{4} * PF * cos(\theta) \quad (2.17)$$

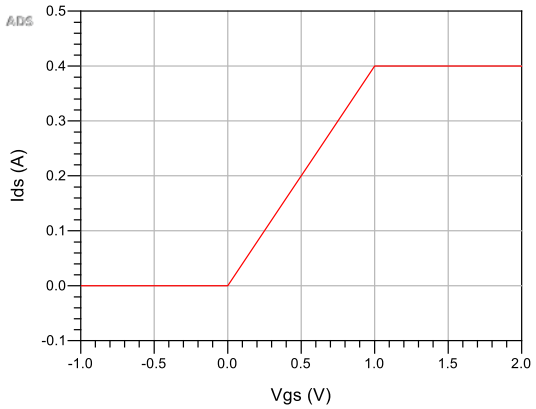

Figure 2.4 – DC drain current versus DC gate voltage of the nonlinear model used to describe the ideal transistor.

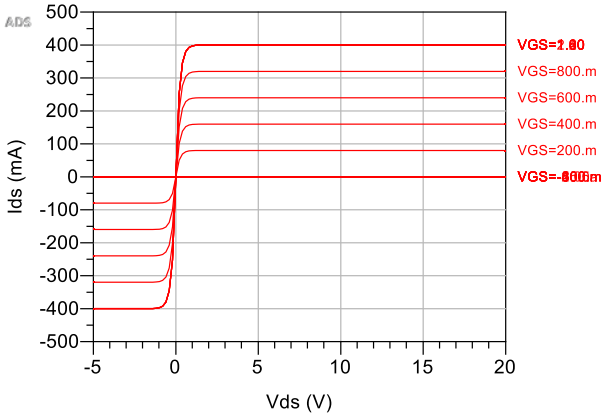

Figure 2.5 – DC IV Curves of the nonlinear model used to describe the ideal transistor

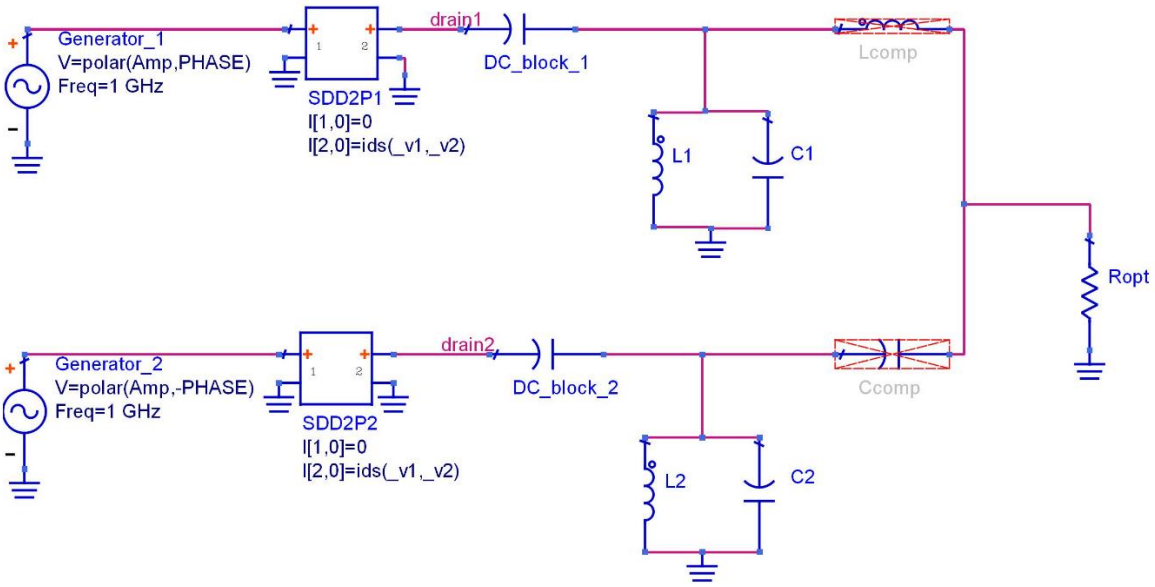

Figure 2.6 - Circuit used to simulate Chireix Combiner with 2 amplifiers operating as a linear class B

In order to validate the equations deduced by the mathematical analysis, the circuit represented in fig. 2.6 was simulated in ADS, sweeping the phase of both generators. Their results, represented in fig. 2.7, show the impedance presented to each PA, varying from the center of the Smith Chart to the Short Circuit, confirming eq. 2.12 and 2.13.

In the same figure, but on the left plot, it can also be seen the total system efficiency, represented with a blue line, as well as the Power Factor of the combiner, represented with a green line.

The PF is being defined because, despite the power is not all delivered to the load, it would not be wasted if some kind of device could retain it. So, some topologies were designed to take advantage of it, converting the RF power to DC power, injecting again in the DC supply [3].

The efficiency plot of fig. 2.7, only evaluates the efficiency of each amplifier with respect to the phase difference. Yet, as this system is being studied to present good efficiency at higher OPBO, a plot representing the efficiency versus the output power is welcome, fig. 2.8.

Looking again to the plots of fig. 2.7, it can be verified that as the phase moves to 90 degrees the efficiency degrades due to the load variations. However, introducing new non dissipative elements in the circuit, as proposed by Chireix, the reactive impedance can be cancelled, optimizing the PF for particular angles, as it will be explained in the next section.

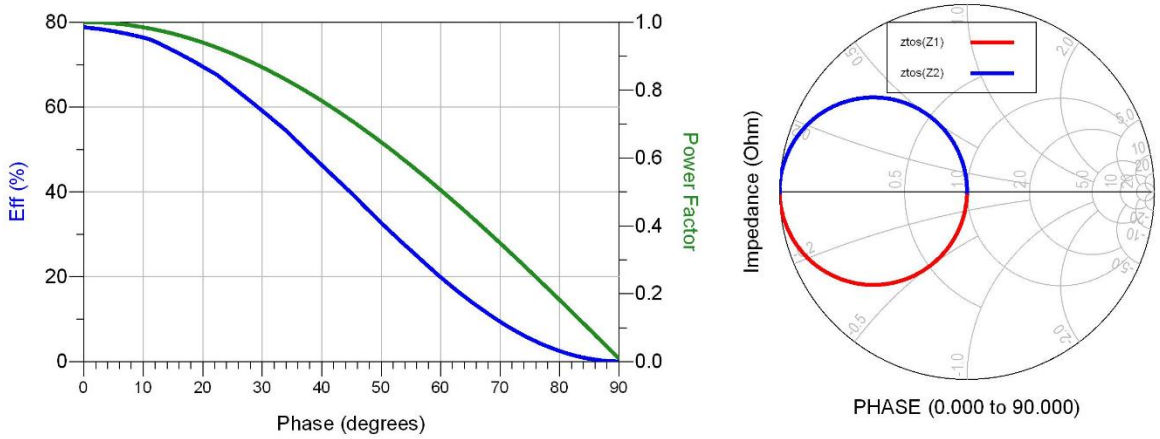

Figure 2.7 – Drain efficiency, Power Factor and impedances represented in the Smith Chart. In the left plot is presented the PF (green line), as well as the system efficiency (blue line). In the right plot it is presented the impedance seen by each amplifier, normalized to 50Ohm.

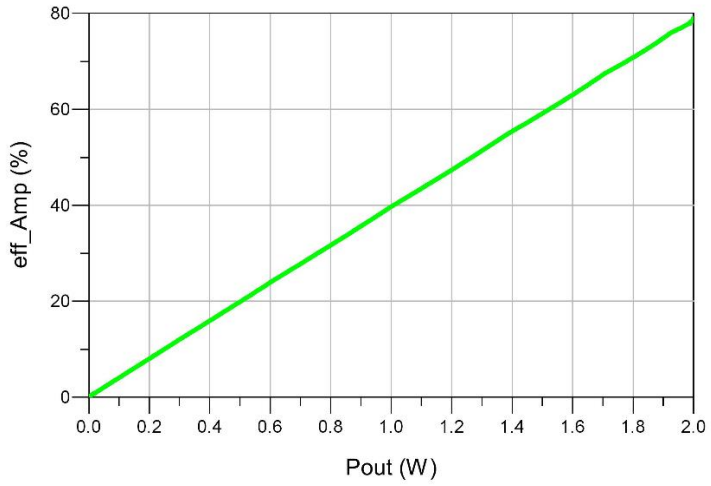

Figure 2.8 – System efficiency versus Output power.

2.3.2. Chireix Amplifier with compensation

By choosing an angle, the reactance presented at each PA can be determined through eq. 2.12 and 2.13, and so, two lumped elements can be added to the circuit in order to cancel the imaginary part. Notice that these elements must be added in series, otherwise the voltage in the drain will not change, since it still is a direct consequence of the current on the load. It is expected that both half-moons observed in the Smith Chart change their position, presenting only real impedance for the chosen angle, as the next fig. 2.9 and 2.10 show, after making the described process for an angle of 15 degrees.

As it can be observed in the Smith Chart, the half-moons have moved, cancelling the imaginary part twice. Looking to fig. 2.9, it can be seen, clearly, in which phase this happens, i.e., when “Power Factor” is equal 1. In fact, the reactive power was reduced and the PAs are seeing a real load for almost all phases. However, in terms of OPBO, this is not much significant, fig. 2.11.

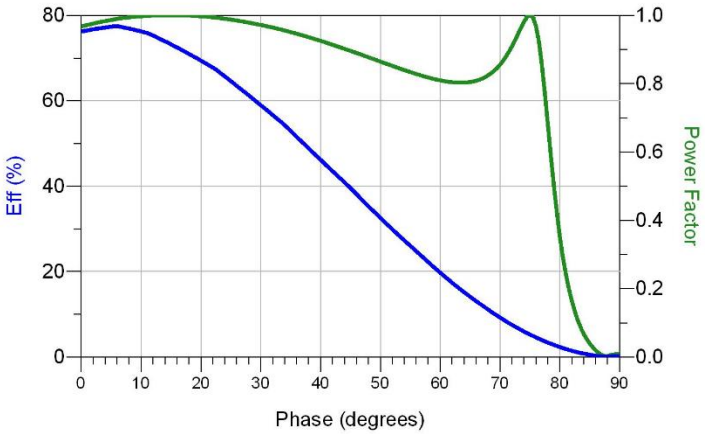

Figure 2.9 – System efficiency and PF metrics using a combiner compensated to 15 degrees.

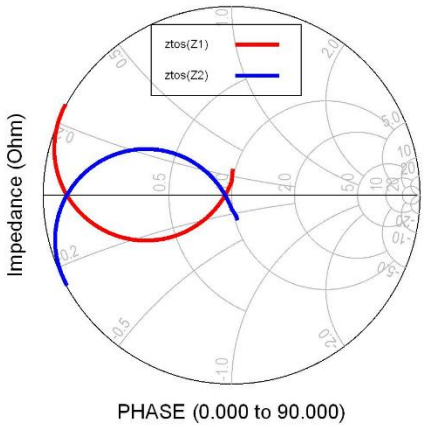

Figure 2.10 - Impedance seen by each amplifier, normalized to 50Ohm, and compensated at 15 degrees

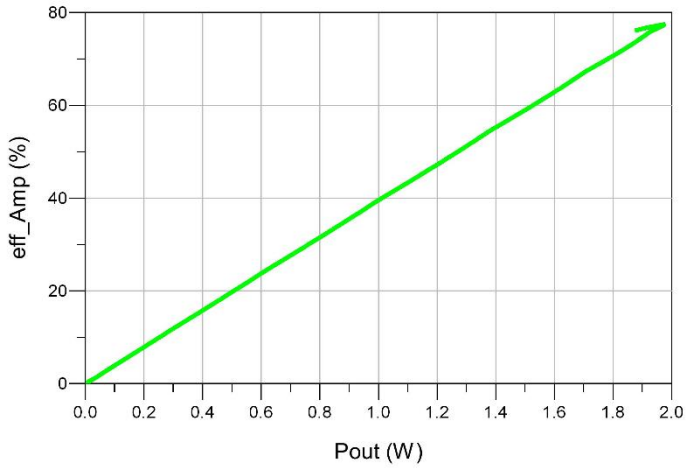

Figure 2.11 – Efficiency versus Output power using a combiner compensated to 15 degrees.

Yet, increasing the compensation angle once more and the knee voltage of the transistor model, the system efficiency is improved for greater OPBO, in spite of the maximum efficiency be reduced as well as the maximum power, fig. 2.12 and 2.13. This can be explained due to the high reactive and real values that the load assumes, simultaneously, which is responsible to keep the voltage drain high but also to reduce the amount of current delivered to the load. In that situation, the transistor is starting to operate as saturated PA, and so, its behaviour is changing from a current source to a voltage source.

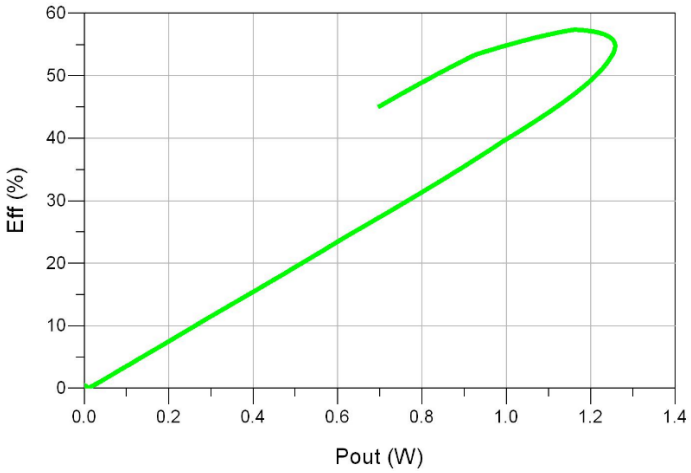

Figure 2.12 – System efficiency when compensated with high reactances and with a greater knee voltage

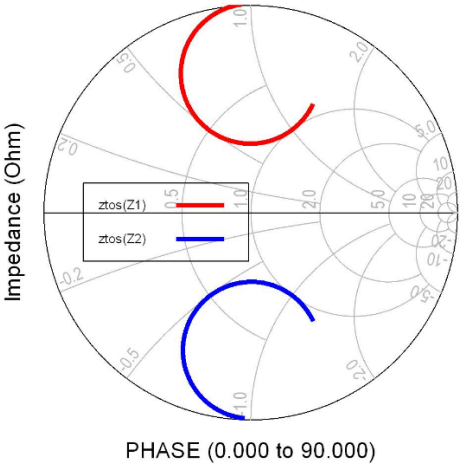

Figure 2.13 – Impedance seen by each amplifier, normalized to 50Ohm, when compensated with high reactances

Due to practical reasons, a transmission line can be added to the circuit, between the PA and the load of each PA path. However, this line must have 180 degrees of length, preserving the circuit behaviour. Dividing this line into two, the compensation can be done through a stub in their midst as represented in fig. 2.14. Notice that the capacitor and the inductor had to be changed and their values calculated again through equations 2.18 and 2.19.

$$Y_1 = \frac{2*R_L}{{Z_0}^2}\left(cos(\theta)^2 - j\frac{sin(2\theta)}{2}\right) \quad (2.18)$$

$$Y_2 = \frac{2*R_L}{{Z_0}^2}\left(cos(\theta)^2 + j\frac{sin(2\theta)}{2}\right) \quad (2.19)$$

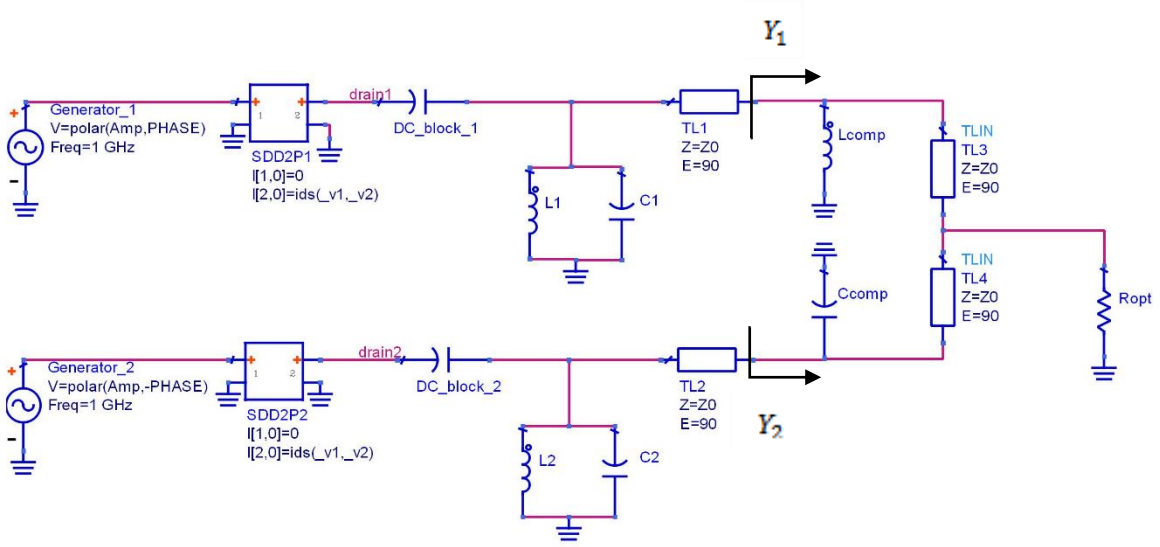

Figure 2.14 - Chireix Combiner compensated with stubs

This chapter has presented an overview about the Chireix Combiner, demonstrating how the input signal can be modulated and how the impedances presented to each PA can be handled. Yet, to take the most of this system, the current provided by the generator has to be reduced according to the reactive impedance presented to it, while the drain voltage has to keep high. In that situation, the power delivered to the load will vary while the efficiency will keep high. So, in the next Chapter it will be studied the behaviour of this system using highly saturated PAs.

3. Testing Chireix with highly efficient Amplifiers

As it was observed in the previous Chapter, the Chireix Combiner imposes a wide range of dynamic loads. So, to improve the efficiency, the PAs that will be used have to present good resilience to load variations. In order to choose the best class of PAs, it was done a study at two powerful classes of operation, Class F and Class E. Although both can achieve good efficiency, their design is based on different concepts and so, it is expectable that they present different behaviours when operating with the Chireix Combiner.

Before starting to discuss the results obtained in simulation, a brief introduction to these classes is going to be presented in order to better understand the results presented by the simulator.

In the end, and after designing one PA for each class, the Chireix Amplifier will be tested.

3.1 Class F

This class of operation is similar to class B, yet, it imposes two more conditions beyond those that define a class B amplifier. Those conditions are to operate in saturation mode and to present pre-defined impedances to the odd harmonics instead of the short circuits.

To achieve a good efficiency in a power amplifier, the overlap between the current and voltage waveforms in the drain has to be reduced. So, in this architecture, this was fulfilled by changing the voltage waveform in the drain. Instead of being a sinusoid, as in the pure class B, the waveform is now a square shape.

Decomposing a square wave in time domain into the frequency domain by the Fourier Series, eq. 3.1 (Appendix B), it is observed that this wave is composed only by odd components. So, to perform that, the transistor has to be saturated, generating odd components, and the impedance presented to them, has to have high values. In the case of even components, the short circuit has to be maintained as in class B, generating the shapes observed in fig. 3.1 (left image).

If it was possible to handle the impedance for a high range of harmonic components, the waveform could be almost square and, in the limit, it could be exactly square. However, in practice, only a small number of harmonics can be handled.

For that reason, this architecture cannot be 100% efficient and is less efficient when lower harmonics are controlled, fig. 3.1 (right image).

$$f(x) = \begin{cases} 0, & x < 0 \\ 1, & x \geq 0 \end{cases}$$

$$F(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty}\left[a_n \cos\left(\frac{n2\pi t}{T}\right) + b_n \sin\left(\frac{n2\pi t}{T}\right)\right] = 0.5 + \frac{2}{\pi}\sin(t) - \frac{2}{3\pi}\sin(3t) + \cdots \quad (3.1)$$

Fourier Series Coefficients:

$$a_n = \frac{2}{T}\int_{-\pi}^{\pi} f(x) * \cos\left(\frac{2\pi n x}{T}\right) dx \quad (3.2)$$

$$b_n = \frac{2}{T}\int_{-\pi}^{\pi} f(x) * \sin\left(\frac{2\pi n x}{T}\right) dx \quad (3.3)$$

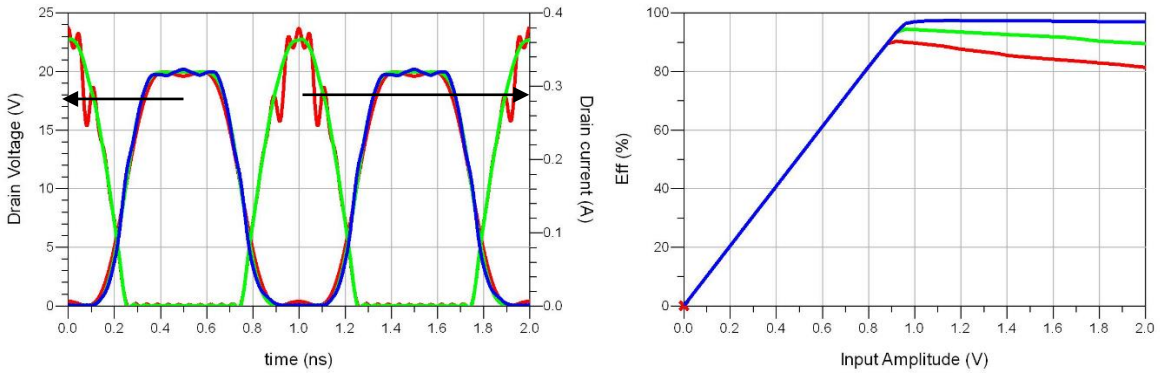

Figure 3.1 – Drain waveforms and respective efficiency of a class F PA. Left image shows the voltage and current waveforms in the transistor drain, while the right image exhibits its efficiency. These plots were obtained doing a sweep on the number of harmonics that are being controlled (3rd – red line, 5th – green line and 7th – blue line).

3.1.1 Designing a class F PA with a real transistor

Implementing this architecture with a real transistor requires more work, to find the optimum impedance at each harmonic. One easy method to do that would be the load pull, in an iterative way for fundamental and harmonic components. However, since a model for the GaN35015 [5] with access to the intrinsic drain was available, better results were reached when the impedances were selected looking directly into the drain waveforms, fig. 3.2. To reach these results, it was used the schematic represented in fig. 3.3. In the input match, it can be seen an RC filter that was used to achieve unconditional stability, as well as the "Z_s_fund" variable used in the source power. This variable is responsible to improve the

gain but, later this will be explained in detail. At the output, an impedance block was used to present the optimal impedances at the fundamental and harmonic components. Since now the amplifier is being simulated with a model that describes a real transistor, which already includes the parasitic effects of the device, the impedance that will be presented to the transistor has to have into account the effects introduced by those parasitic elements. In other words, a short circuit on the extrinsic drain does not ensure a short circuit on the intrinsic drain.

In the limit, this Amplifier can be described as a switch amplifier, since when it is conducting it does not have voltage and vice versa. However, the authors reserved this name just for the amplifiers operating in class D or E mode.

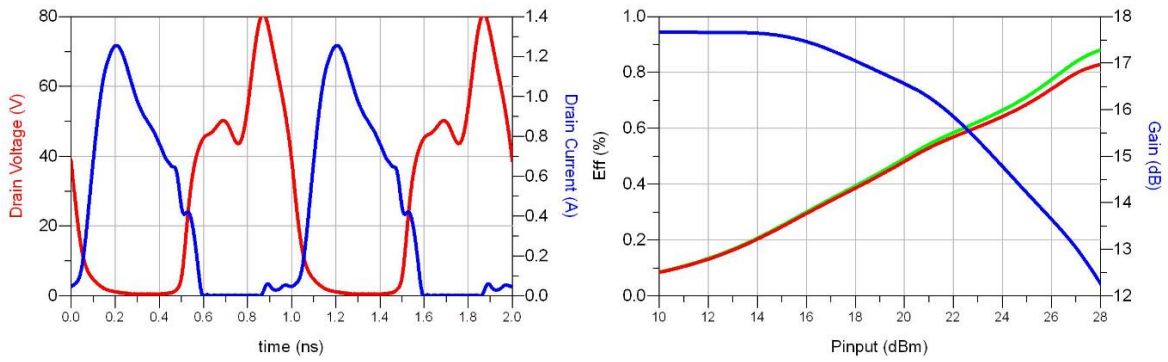

Figure 3.2 – Drain waveforms and efficiency for the designed class F PA with GaN HEMT CGH35015 transistor. Right plot represents the simulated results obtained for efficiency (green), PAE (red) and Gain (blue) while the left plot shows the voltage (red) and current (blue) waveforms in the intrinsic drain.

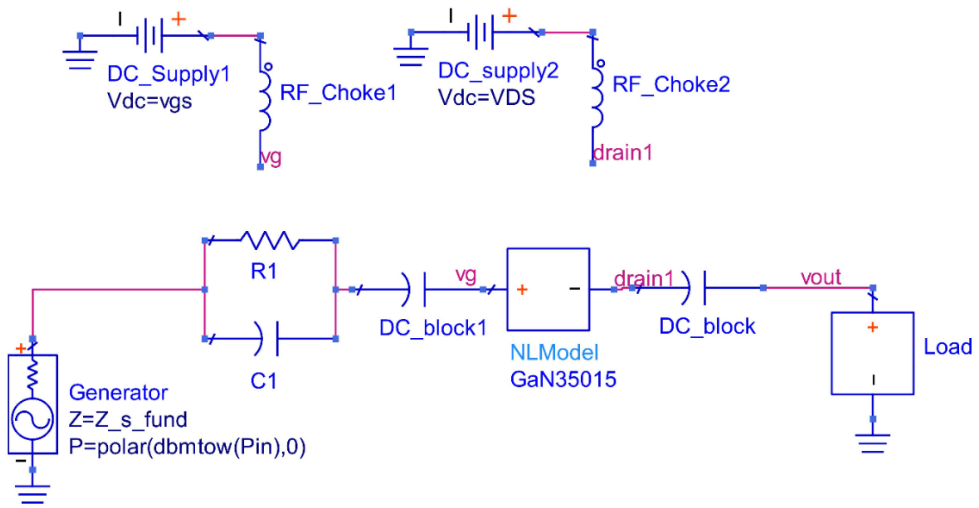

Figure 3.3 – Schematic used to simulate the class F PA using Cree CGH35015 transistor.

3.2 Class E

Class E architecture derives from class D amplifiers, in which both transistors operate alternately, fig. 3.4 (left plot). In the case of class D architecture, a second transistor is used to allow the current to keep flowing when the first transistor is cut off. Since the waveform in the drain has to remain square, the only way to filter it is by adding a LC filter in series with the configuration used in fig. 3.4 (left plot) or similar, forcing the current to flow always by one of the active devices. At higher frequencies, and when the first transistor is cut off, the current can keep flowing throw a capacitor, C_{DS} in this case, avoiding the need of a second transistor and at the same time eliminating the power dissipated on it, fig. 3.4 (right plot).

So, when the transistor is conducting, the current flows through it and the voltage goes to zero, ideally. However, when it is cut off, the current can only flow by C_{DS}, forcing the drain voltage to raise or to decrease depending on the current direction, fig. 3.6. In the next cycle, when the transistor starts to conduct again and if C_{DS} is charged, the current will flow from C_{DS} to the transistor, overlapping the current with the voltage. So it's good practice to turn on the transistor only when the capacitor is discharged.

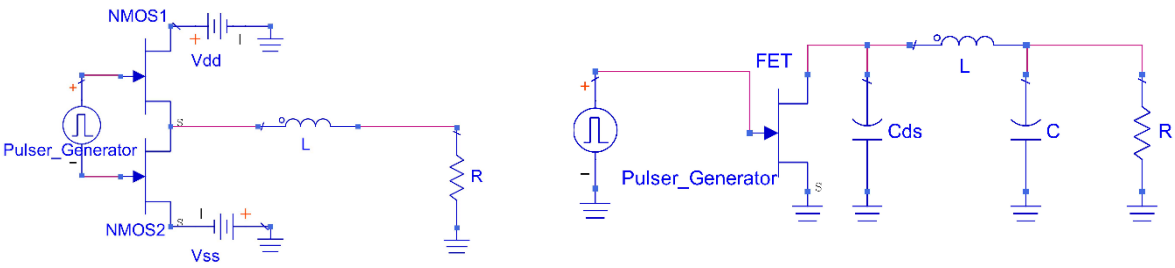

Figure 3.4 – Class D Architecture (left image) and class E architecture (right image).

After this brief introduction to the way how the class E PA operates, the reasoning used in Steve Cripps book [2] was followed to calculate the elements described in the circuit of fig. 3.5, L_{comp} and the $load$ and also the value to the voltage supply, Vdd, for a conduction angle of 150 degrees. This angle was chosen to not exceed too much the drain voltage, providing at the same time enough power to the load.

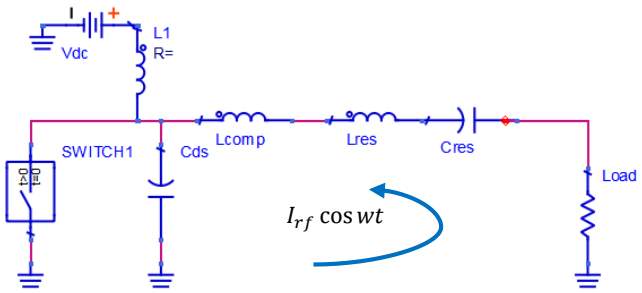

Figure 3.5 – Class E architecture

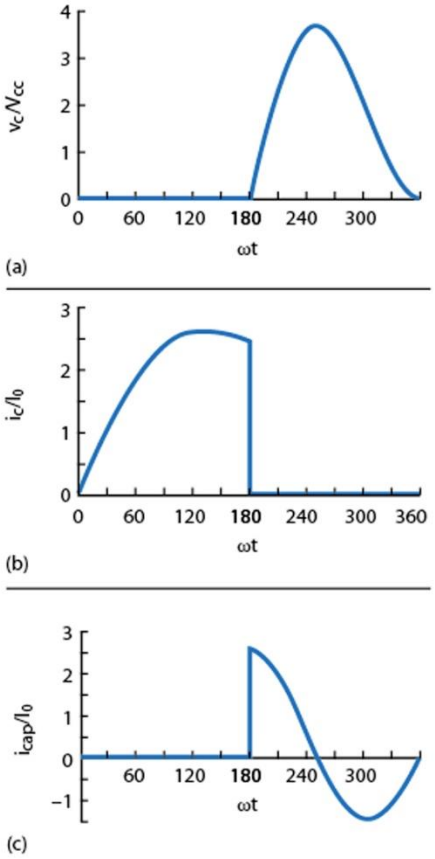

Figure 3.6 – Class E, ideal waveforms, http://www.microwavejournal.com/legacy_assets/FigureImg/AR_3096_F6.jpg

To validate these results, a class E schematic was designed, using again the nonlinear model referred previously when the class F PA was designed, obtaining the following values: V_{DC} = 7.4V; R_L = 44Ohm; L = 7.5nH with a pre-defined conduction angle of 150 degrees. From the mathematical analysis, it was expected to obtain a final value of 0.585W for Pout, 21V to the drain voltage and a current on the load of 0.163A, fig. 3.7.

After the simulation in ADS, it was observed that the current on the load fell below than 0.14A, fig 3.7, delivering no more than 0.4W, fig. 3.8 and so, the supply voltage had to be increased for 8.3V, forcing the current to raise up to 0.163A.

Comparing the waveforms in fig. 3.7 with those represented in fig. 3.6, there are no doubts that the amplifier is operating in class E mode. Furthermore, it can be concluded that the analysis done in time domain was capable to predict, satisfactorily, the current and voltage values in the circuit and therefore, determine the values of the inductance, resistance and DC Voltage. In the next figure, fig. 3.8, it can be seen also that the Amplifier was well designed, presenting good efficiency.

As the results obtained were reasonable well predicted, the method used to design this amplifier with a nonlinear model will now be used to design this time, a class E PA with a real transistor.

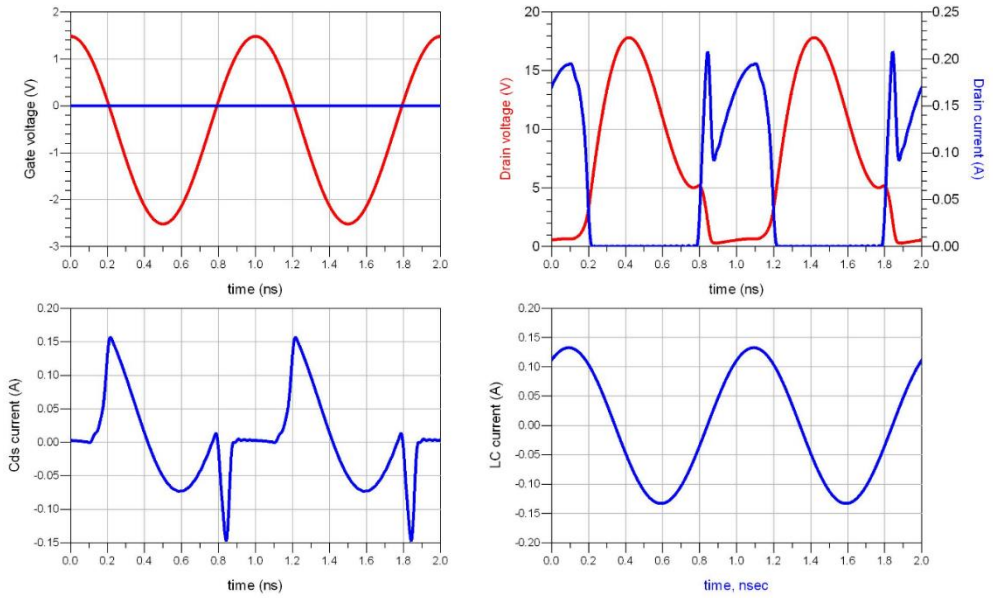

Figure 3.7 – Waveforms for the designed class E amplifier using a nonlinear model and operating at 1GHz, V_{DC} = 7.4V; R_L = 44Ohm; L_{comp} = 7.5nH and a conduction angle of 150 degrees.

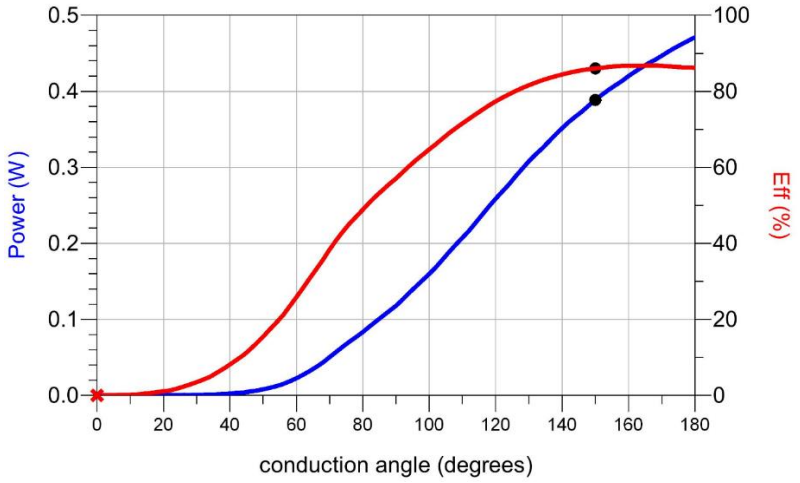

Figure 3.8 – Power delivered to the Load and respective efficiency.

3.2.1 Designing class E PA with a real transistor

So, following the same process, but now considering the Cree GaN35015 HEMT as the transistor, new values for the $load$, $Lcomp$ and V_{DC} were calculated. However, they are very similar to the previous ones, since the frequency and C_{DS} are the same and the loadline does not vary too much, eq. 3.4 and 2.14.

$$R_{opt} = \frac{2*V_{DD}}{I_{max}} = \frac{2*28}{1} = 56\ ohms \tag{3.4}$$

In the next figure, fig. 3.9, it can be seen that the results obtained using the lumped elements calculated by the previously method are very useful as a first approximation. However, to increase the output power it is required to lower the inductance of compensation, having direct impact on the power dissipated in the drain. Once again, the current in the drain presents a different shape from the ideal, which can be justified by the presence of harmonic components in the current. This performance could be improved if the magnitude and phase of the harmonic components were manipulated, changing the impedances presented to it, or even by adding more frequency components at the input signal. Yet, for now, since the objective is just to implement a Chireix Amplifier and not the best Class E Power Amplifier, it is not necessary to go into more detail.

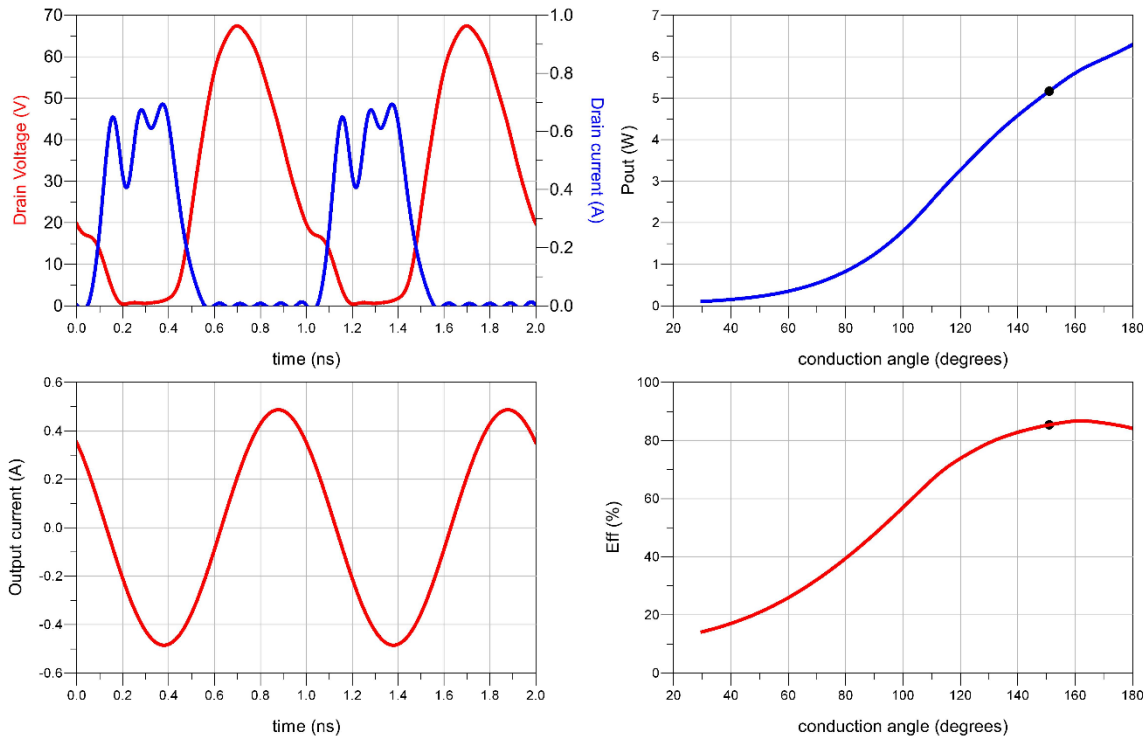

Figure 3.9 – Class E behaviour with a real transistor. These plots are related to the class E amplifier designed with GaN35015 with lumped components. The first plot at left shows the voltage and current waveforms in the drain. Below that, is represented the current at the output and the plots at the right present the Power delivered to the load and the efficiency of the PA.

3.3 Chireix Combiner using highly efficient PAs

Since PAs are already designed, it is time to place them to operate together as an Outphasing system, through a Chireix combiner. The Combiner was already studied in Chapter 2 and it was concluded that the impedance presented to the PAs depends also on the Combiner parameters. So, it has to be designed according to the optimal impedance of each PA and equations 2.8 and 2.9, which relate the line impedance with the load of the combiner.

3.3.1 Chireix Class F

Starting with the designed class F PA, a proper combiner has to be designed, fulfilling the requirements for its optimal impedance. So, the impedance line and the load on the output of the combiner have to be determined, satisfying the optimal impedance of each PA, which is around 50 ohms. There are multiple combinations that can satisfy this condition. However, to simplify it, both Z_0 and R_L will assume equal values. Now, as the equations have just one variable, they can be solved, reaching the conclusion that Z_0 has to be always twice than the optimal impedance of the PA.

Figure 3.10 shows the schematic that was used to simulate the Chireix amplifier with two PAs operating in class F, which are equal to the ones previously designed. Considering that the load of this combiner will be purely resistive, the matching of the imaginary part of both PAs has to be done in their output matches. In this schematic, this was done through the Z1P2 and Z1P3 blocks. Z1P4 and Z1P5 blocks work just as a resonator, ensuring that, at this point, the impedances presented to the harmonics are always a short circuit. Therefore, the impedance presented to the PA output only affects the fundamental component. It should be highlighted that, instead of the common capacitor and inductance that were used to make the compensation of the Chireix Combiner, a single variable to adjust the line length of TL1 and TL2 is now used. This variable increases the line length of the top amplifier and decreases the one of the in bottom amplifier, creating the same impact as if an inductance and a capacitance were used [7].

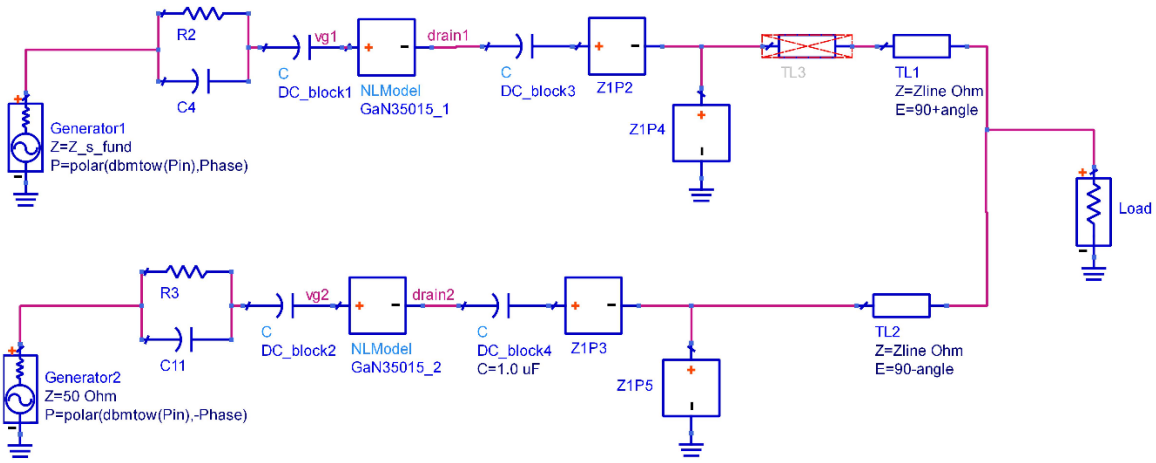

Figure 3.10 – Schematic used to simulate Chireix Combiner with a pair of Amplifiers operating in class F.

Looking to the next Smith Chart, fig. 3.11 , it can be observed the impedances presented in each PA. The first thing that stands out is the assymetry between both lines. Until now, these lines were always symmetrical, since it was used a nonlinear model having no parasitic elements. Yet, this model had to be substituted by one capable of representing the HEMT GaN 35015 transistor having a complex optimal impedance. Thus, a reactive value was added to Z1P2 and Z1P3 blocks, ensuring that after the proper real load be applied to the PAs through the combiner, they will see the optimal impedance for the maximum output power. This step made this system assymetrical, because in practice, 2 inductances were added in the path between the transistor and the Combiner. Furthermore, for the case of the amplifier that is subjected to the reactive load from the Combiner, it is possible to observe that it will never cross the x axis, i.e., the impedance presented to it will be always reactive.

It can also be noted that in its intersection, they have the maximum power and the efficency is lower than the results obtained for a class F PA. This is a direct consequence from the load pull contours, in which the load that gives the maximum output power is a bit far from the load that gives the maximum efficiency, fig. 3.12. Moving away from this load causes a reduction in the power delivered. Yet, the efficiency can decrease or increase depending on the course of this dynamic load. In this case, the efficiency is dropping.

In the schematic referred previously, fig. 3.10, a transmission line was short circuited, TL3, yet, this transmission line can be used to handle the course of these line impedances observed in Smith Chart, fig. 3.13. Although the impedance presented to each PA is moving

away from the impedance that gives the maximum power, the efficiency raises during a while, to fall again later.

This inherent characteristic to the PAs can be exploited to keep the efficiency high while the power delivered to the load varies. So, if the objective is to achieve the maximum efficiency at 5 dB of OPBO, the wiser action to pursue is to choose a transistor or change the frequency, such that the load that gives this power is crossing the load that gives the maximum efficiency. Probably, changing the impedances presented to the harmonics can be a away to change the load pull contours at the fundamental component.

In the next topic it will be demonstrated that this technique of handling the line impedances will improve a lot the Chireix Combiner with class E PAs.

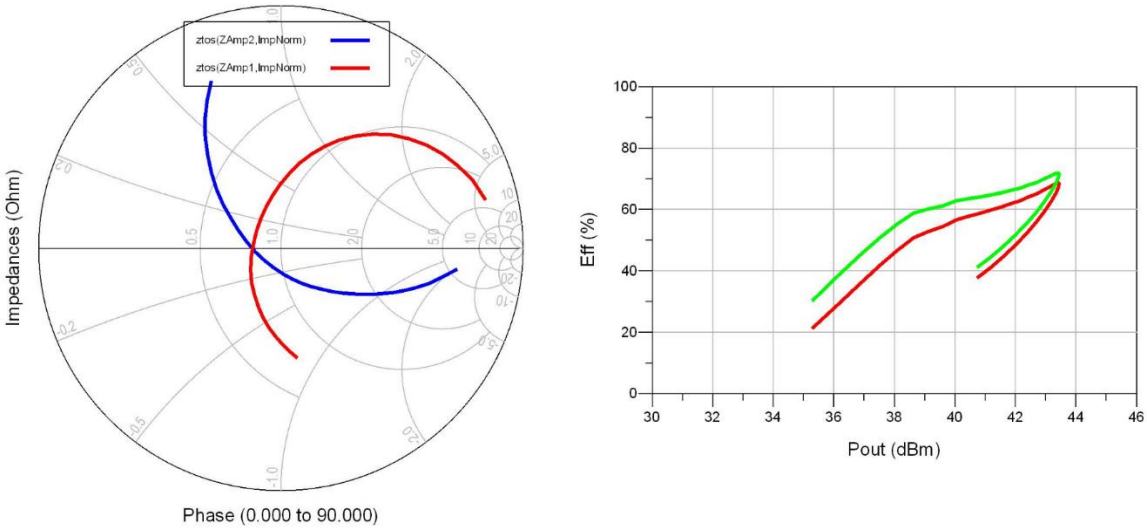

Figure 3.11 – Compensated Chireix Combiner operating with class F PAs. Left plot shows the impedances presented to each PA and the right plot shows the system efficiency (drain efficiency – green), (PAE - red).

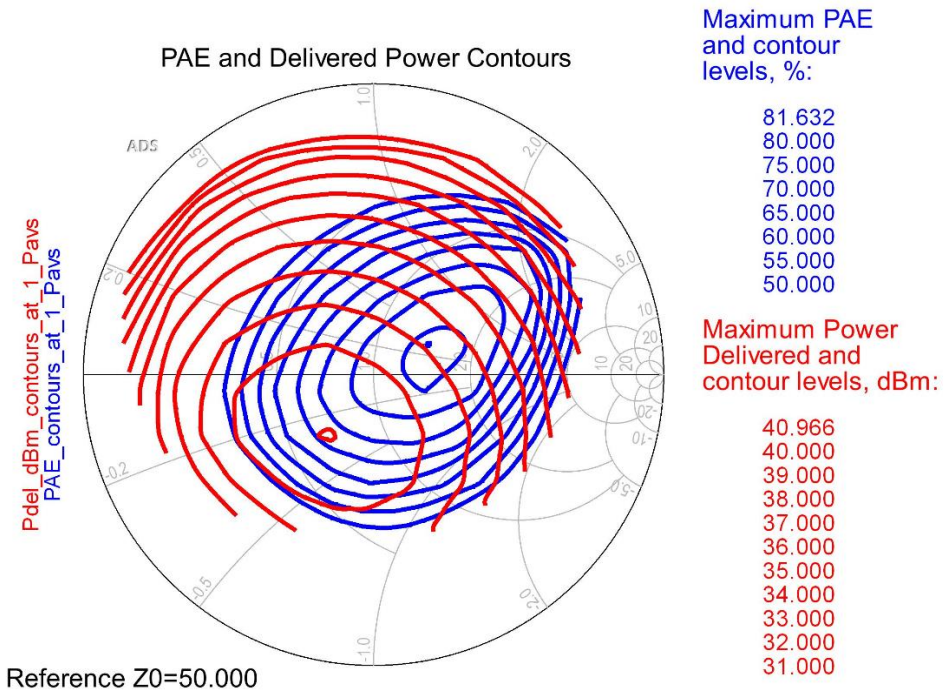

Figure 3.12 – Load Pull contours for the fundamental component of the class F PA.

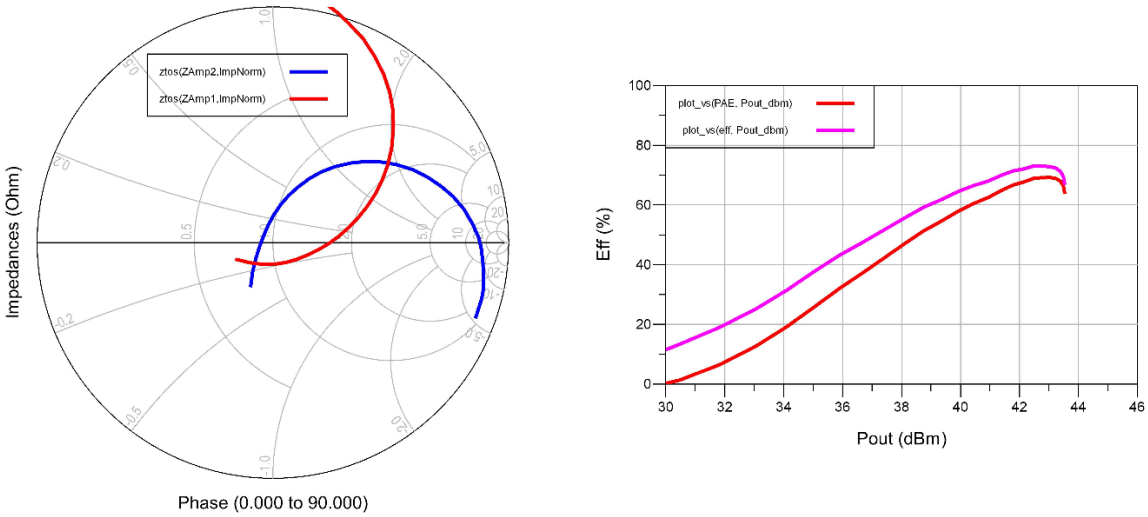

Figure 3.13 – Compensated Chireix Combiner with class F PAs and aided by a transmission line to handle the impedances path presented to each PA.

3.3.2. Chireix Class E

With the purpose to do the same study, but now using class E PAs, a new Chireix Combiner was designed having into account that the optimal impedance of the class E PA is different. The schematic represented in fig 3.14 shows the final configuration. It is similar to the schematic used for the designed class E PA, but with two transmission lines in the end, forming the Chireix Combiner.

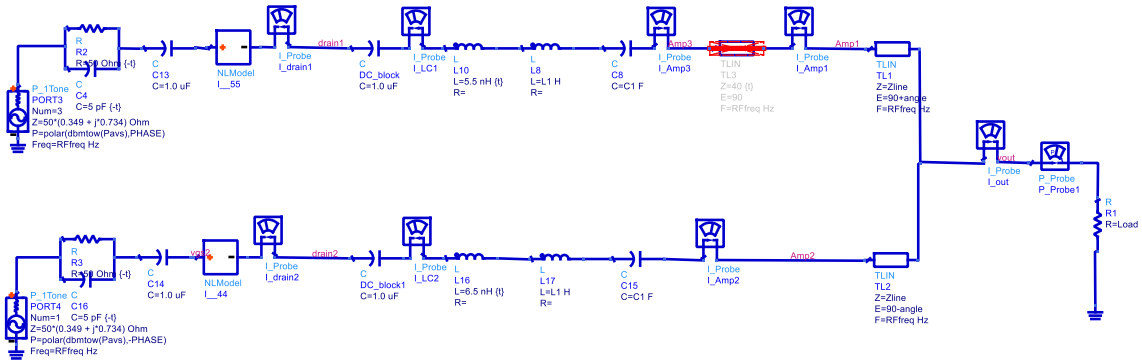

Figure 3.14 – Compensated Chireix Combiner operating with Class E PAs.

Some publications have report good results for this configuration, yet, this was not the case for this schematic after the simulation, fig. 3.15. In order to understand these poor results, the load pull of the class E PA designed had to be analysed, fig. 3.16. Comparing this figure with the Smith Chart in fig 3.15, it can be seen that the impedance presented to the PAs is going to regions where the PA has low efficiency. So, in order to fix it, the same line added in class F Chireix Combiner was also added to this schematic, with different electric length, forcing the path of those impedances to cross desired regions. The results could not be more satisfactory, fig. 3.17. Not only the output power increased as the drain efficiency kept high during more OPBO, represented in blue line. Now, only the PAE compromises these so promising results. When the PA was designed, a RC filter was added to the input match to keep it always stable. However, this filter can be changed for achieving higher gain and, for that, it is only needed to increase the resistor value. After doing that, and since the gain was improved, the input power of each PA had to be reduced in proportion to the gain increase, generating a new curve for the PAE, fig. 3.18. Having in mind all this process and for these implemented PAs, hardly, with a Chireix Combiner and using Outphasing concept, the efficiency can be improved.

To sum up, the main characteristics that a PA using a Chireix Combiner should be concerned are the maximum gain of each transistor and the relation between the PAE and Power delivered Contours. Probably, for the designed class E PA, these contours couldn't be better localized. Notice that in fig. 3.16, by the Load Pull Contours, it can be observed that the load that gives the maximum efficiency is 4dB away from the load that gives the maximum power. By other side, in fig. 3.12, the load that gives the maximum efficiency, is only 2 dB away from the load that gives the maximum power. Besides that, the PAE Contours of fig. 3.12 are smaller than the PAE Contours of fig. 3.16, explaining the poor results obtained for Chireix Amplifier designed with class F PAs. To reject completely the class F architecture, other transistors should be evaluated or this transistor should be tested for other frequencies.

Since the results obtained for the designed Chireix Amplifier with class E PAs are, by far, much better, the next Chapter will explain how this system can be implemented with them, in order to verify these exciting results in a practical system.

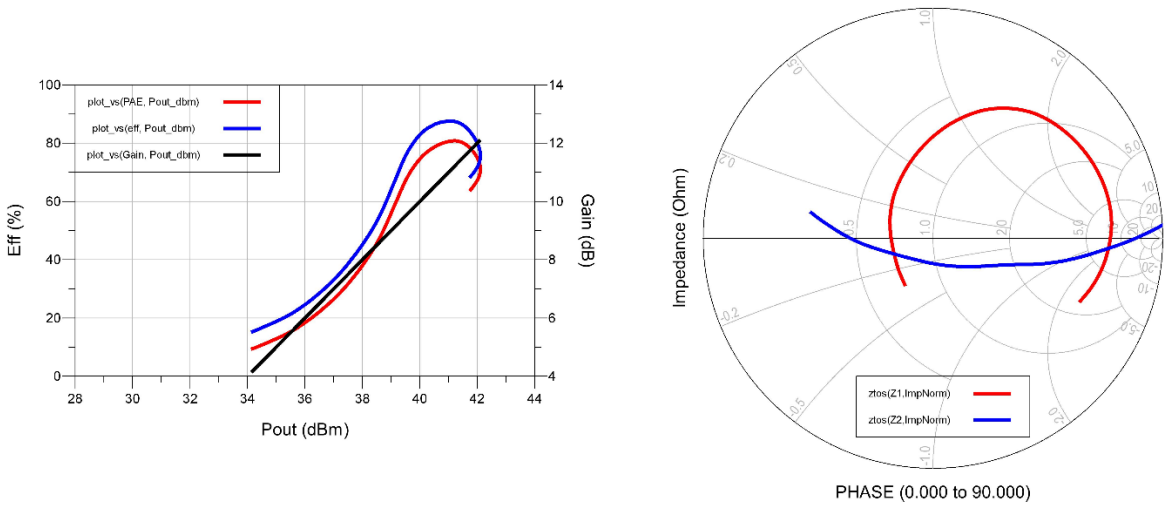

Figure 3.15 – Results obtained for the first Chireix Amplifier designed with Class E PAs.

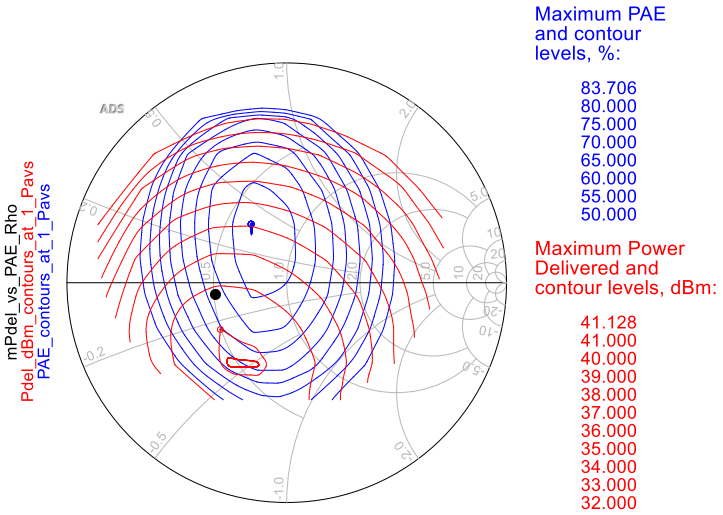

Figure 3.16 - Load Pull contours for the designed class E PA.

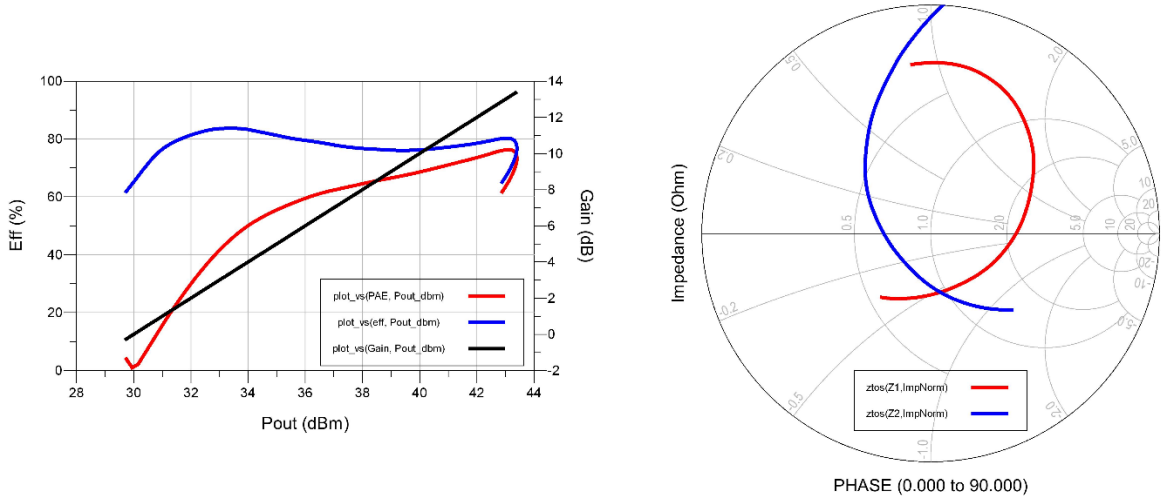

Figure 3.17 – Results obtained for the designed Chireix Amplifier after to handle the path of the line impedances with an extra transmission line.

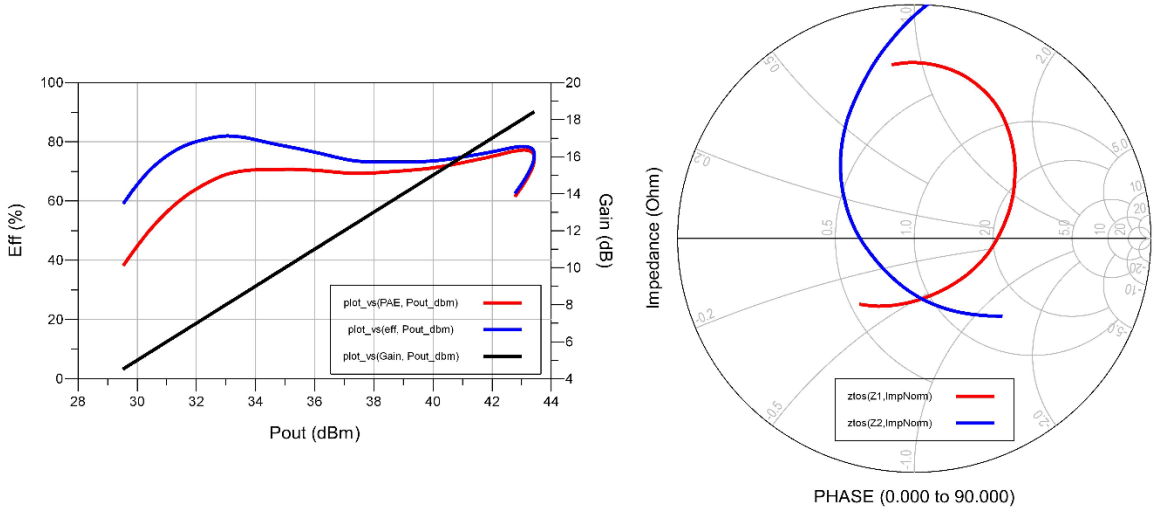

Figure 3.18 – Results obtained for the designed Chireix Amplifier after being added the transmission line and its gain improved.

4. Chireix Implementation with Class E Amplifiers operating at 1.8 GHz

Until now, the frequency used to study the Chireix Combiner was 1GHz but from now on, a new frequency of 1.8 GHz is going to be used. This change is due to hardware limitations in the laboratory and to take advantage of a model built in Aveiro University, which provides access to the intrinsic drain. This means that a new class E PA has to be designed.
So, this Chapter starts to present the load pull contours for the new class E PA designed to then, implement it with transmission lines. By the end, this new amplifier will be replicated forming the Chireix Amplifier.

4.1 Class E (lumped elements)

Since the frequency was changed, the class E PA of the previous Chapter has to be redesigned. So, using again the same reason described in Steve Cripps book's, new values for the components were calculated. In fig. 4.1, it can be seen the waveforms in the drain and the load pull contours at the output of the amplifier. Comparing these Load Pull Contours with those obtained for the Class E PA at 1 GHz, fig. 3.20, it appears that the load that gives the maximum power is closer to the load that gives the maximum PAE and the region of the maximum PAE is smaller. So, taking into account these factors, it is predictable that a Chireix Combiner designed with this PA will have worst ratio between OPBO and PAE.

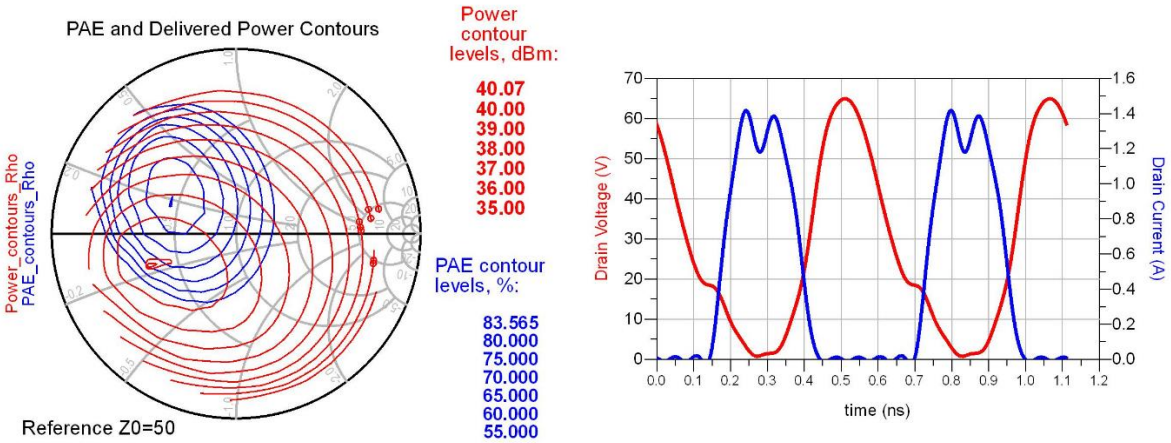

Figure 4.1 – Load Pull Contours and waveforms in the drain for the designed Class E PA fed through a RF Choke.

4.2 Class E (substituting the RF Choke by a transmission line)

It is good practice to design the PAs at these frequencies with transmission lines instead of lumped components, not only because of the losses on these components but also due to their hard characterization at harmonic frequencies. In terms of design, this is also a huge advantage, since it is possible to change the layout to achieve physical compatibilities between the matches of each PA. Another interesting problem is the impedance presented to the envelope signal, that in case of being different from a short circuit can introduce memory effects, inducing distortion in the system [25].

If any other Amplifier class was used, the process would be quite easy. However, in this topology, the way the amplifier is fed in the output has to be carefully thought out. The analysis done to determine the components to be used in the class E Amplifier has considered that the impedances presented to the harmonic components in the drain were only due to the parasitic, C_{DS}. Yet, since the RF Choke has to be substituted by a transmission line and it is impossible to present an Open Circuit (O.C.) through it to odd and even harmonics at the same time, a compromise between those impedances has to be achieved. In the case of the fundamental component, the output match can compensate any deviation on the ideal impedance.

To solve that, the length of transmission line added in the place of the RF Choke was tuned and for each length, the PAE was measured until the best one was found, fig. 4.2. Although those impedances at harmonic frequencies were changed, the PA still behaves closer to the class E architecture, according to the waveforms represented in the same figure.

In fact, there is a topology capable to present an O.C to 2nd and 3rd harmonics through a combination of transmission lines [6]. However, since the objective is to design a highly efficient PA, the solution found is quite good, at least in terms of the maximum PAE.

Nevertheless, the load pull contours have changed its position and the area of PAE contours has decreased significantly, making it more susceptible to small deviations.

In both Smith Charts, fig. 4.1 and 4.2, the power delivered by the PA at maximum PAE is about 3 dB below than the maximum power, yet it is noteworthy that this relation between PAE and Power delivered can be handled according to the impedance presented to the harmonic components, although it is not observable in these figures. So, a careful design could be followed having in mind this little detail. At this point, the question is not what is the most efficient design, but which of them has the best PAE when different loads are presented at its output, increasing the ratio between the PAE and the OPBO.

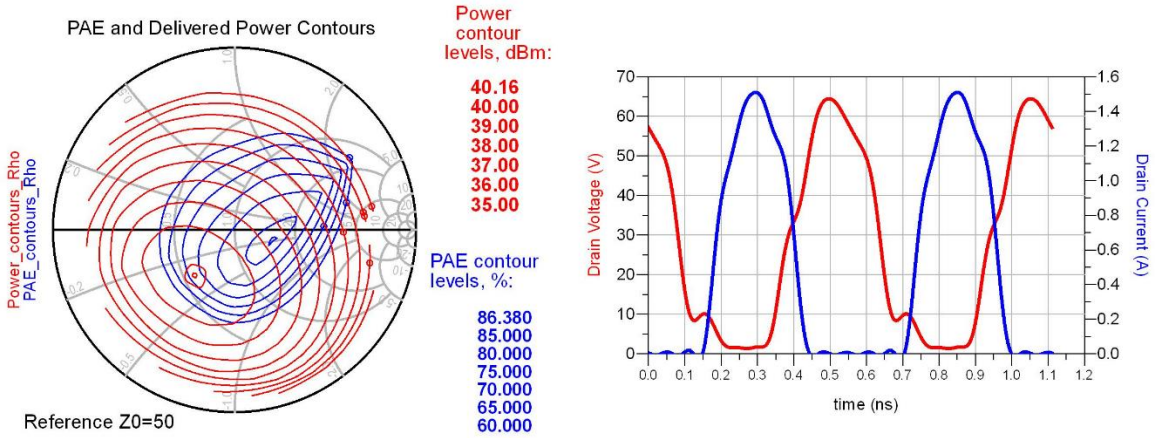

Figure 4.2 – Load Pull Contours and waveforms in the drain for the designed Class E PA fed by a transmission line.

4.3 Input Matching Network Design

So far, the only reference made to the input match was the RC filter in the previous Chapter. Yet, all these designed PAs were adapted at its input otherwise, the PAE could not reach so high values.

To achieve a good gain between the Vector Signal Generator (VSG) and the power at the transistor drain, available power gain, the input match has to present an impedance to the transistor that is the conjugate of its input impedance, adapting it to 50 ohms, internal impedance of VSG.

This conjugate impedance should present the maximum gain, yet, an important condition has to be verified - stability. If the objective was just to design a normal PA with a constant load, this condition would be more easily achieved, yet, in this topology, a small change in one of the matches will have direct impact on the other PA behaviour. Moreover, since the load presented to each PA will change dynamically, it is better to ensure that each PA will always be stable, regardless of the load presented to it.

As suggested by the manufacturer, a RC filter was used to achieve unconditional stability at higher frequencies, but in this case it was used between the input match and the gate. Using this configuration, it is possible to ensure unconditional stability, at least at high frequencies, having total freedom to design the input match. To achieve unconditional stability at lower frequencies it was needed to add a resistor between the gate and DC supply. The input matching network was designed and optimized to present a reasonable bandwidth. However, there is always a compromise between it and the gain. In Fig. 4.3

(right plot), it can be seen the gain achieved for the input match designed when a load of 50 Ohm was presented to the output. In the same figure, on the left side, two functions are plotted, stab_meas() and stab_fact(), proving unconditional stability for this system when it is excited with small signal for a certain range of frequencies. These two functions come from the Rollet Stability Factor and are already created in ADS simulator, meaning that if stab_meas() is positive and stab_fact() is greater than unity, the system is always stable. In figure 4.4, are shown the same results but with the difference that, in this case, the system is being excited with a large signal.

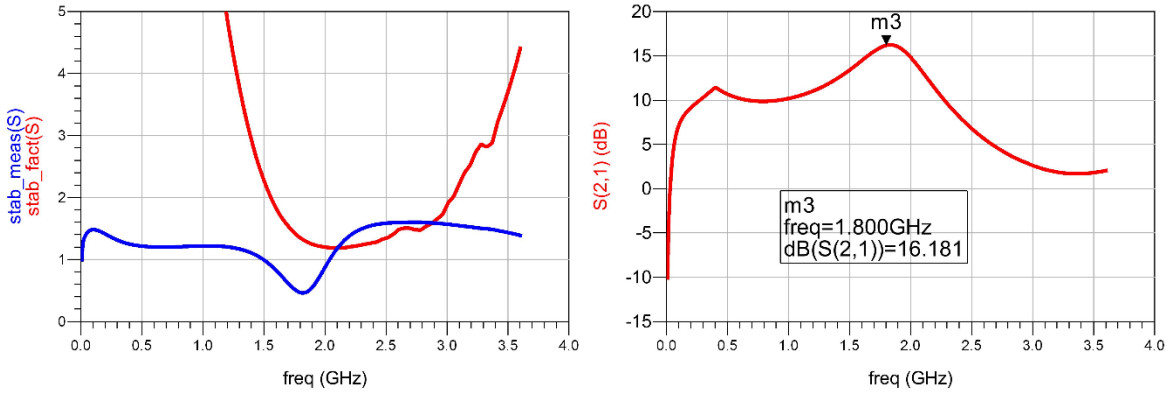

Figure 4.3 – Representation of the Stability (left plot) and Gain (right plot) when the system was excited with small signal – S-parameters

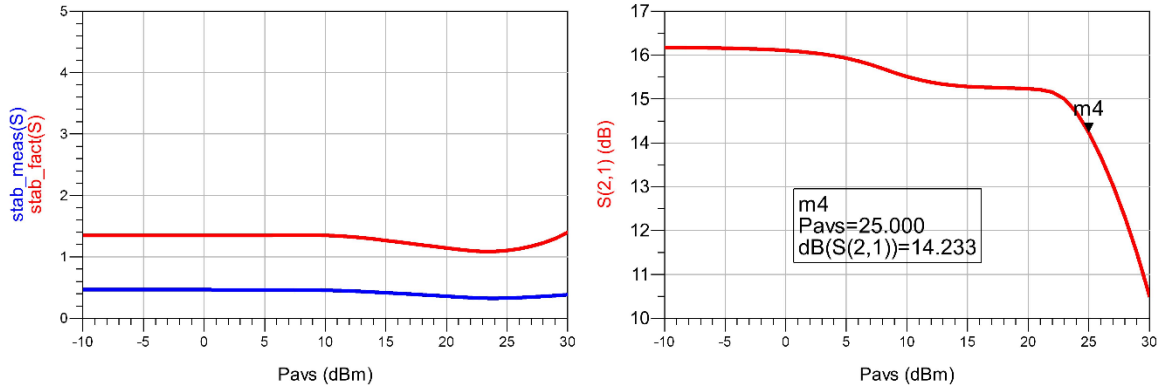

Figure 4.4 – Representation of the Stability (left plot) and Gain (right plot) when the system was excited with a large signal – S-parameters

By making the system always stable, it now has a limited maximum gain. However, after designing the output match and the respective Combiner, the resistor in RC filter can be adjusted to increase the gain, keeping it stable for a certain load at the system output, 50 Ohm normally. Although the load that will be presented to this Amplifier will vary when it will be operating as a Chireix Combiner, only a 50 Ohm load at each PA output was considered.

So, knowing that this load influences the input match, a new improvement can be considered after the Chireix Combiner is designed. In figure 4.5, it can be seen the final layout of the input match without the lumped elements welded. This representation considers that the VSG will be connected at the left, Voltage supply on the top and transistor gate on the right. It has to be highlighted that, in contrary to the simulator, the voltage supply that will be connected to the circuit is not a short circuit. Therefore, and in order to have a reference point, a short circuit has to be provided in the line that goes to the voltage supply. In this case, this short circuit was done with a capacitor in the end of the line. The spaces between the lines are to be fulfilled with lumped elements, ensuring DC isolation between VSG and DC supply and unconditional stability to all frequencies, through the series resistor to the DC supply and the RC filter before the gate. Those two lines between the RC filter and the gate have to have a minimum length of 8 mm, since the transistor will be pressed with a small piece of Teflon creating the electric contact between the transmission line and the transistor gate. At the same time, it will improve the ground around the transistor, since this piece will be screwed to an aluminium base, which, in turn, is contacting the ground plane of the substrate.

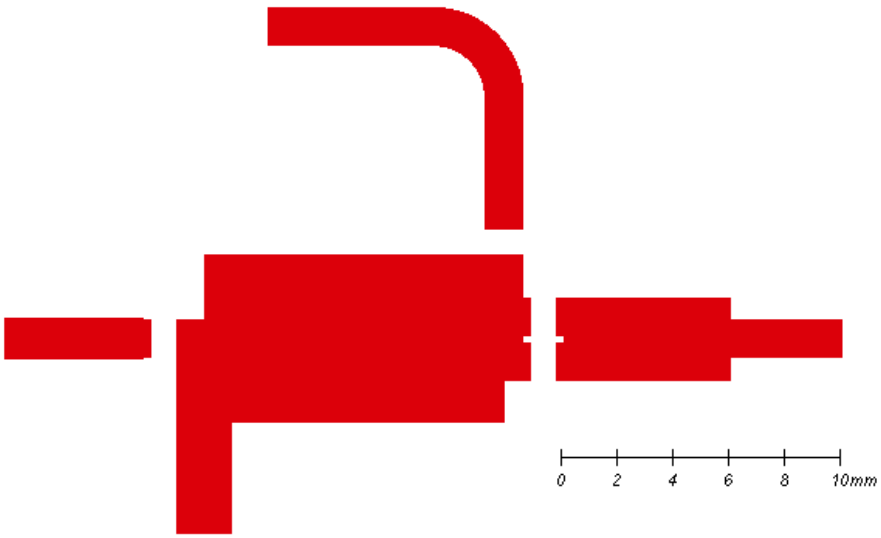

Figure 4.5 – Final RF layout - input matching network

4.4 Output Matching Network Design

In the previous Chapter, it was explained carefully how a class E PA could be implemented with lumped elements. Then in the begin of this Chapter it was studied the impact of substituting the RF Choke by a transmission line. So, to implement the output match with transmission lines, it is only needed now to design a matching network, capable of filtering all harmonic components generated by the transistor to the output, with exception of the fundamental. On the other hand, it was seen that to reach good efficiency, the overlap between current and voltage in the drain, caused mainly by intrinsic C_{DS}, has to be compensated. So, since the impedances that have to be presented at fundamental and harmonic components are already known, a topology to this output match can be predicted to then, use the simulator to determine the length and width of each microstrip line.

The next figure, fig. 4.6, shows the initial topology of the output match that was used to achieve the impedances desired, through the Optimizer ADS tool whereupon, the effect of the transitions between the lines and the s-parameters of the decoupling capacitor are included. The microstrip line TL72 represents the already studied line for the DC voltage supply, TL71 stands for the inductance of compensation and TL75/76 are responsible to implement the pass band filter to the carrier frequency. In the end, another transmission line was added, TL78, with the purpose to convert a load of 50 ohms to the desired impedance. Later on, this line can be substituted by the Chireix Combiner.

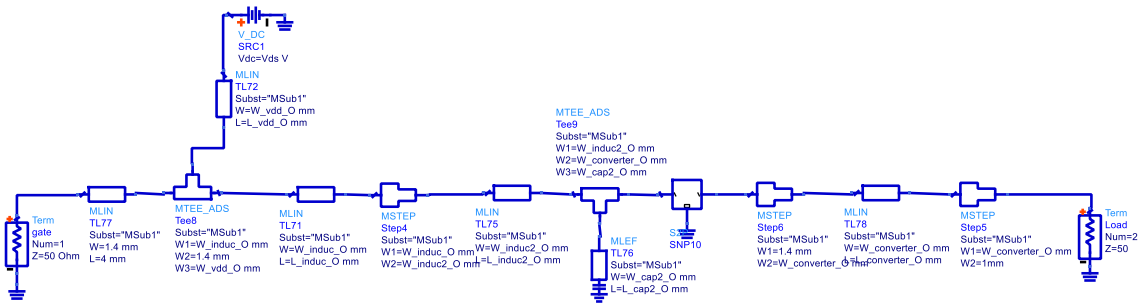

Figure 4.6 – Schematic of the Output Matching Network in the early stage.

To sum up, this output matching network for the class E PA has to present a high reflection coefficient at harmonic components in direction to the load, fig. 4.7, and in the drain it has to present the optimal impedance for the fundamental and harmonic components that maximizes the PAE, fig 4.8. Comparing the load pull contours of this designed amplifier with the amplifier designed with lumped elements, fig 4.9, it can be seen a fall back on PAE greater than 10%. Although microstrip lines are lossy, the main reason to this drop is the

different impedance values presented to the drain at the 2nd harmonic, fig. 4.8. From figure 4.9, right plot, it can be noticed that the impedance that gives higher PAE is a bit far from the center of the Smith Chart. This change can be justified, mainly, by the displacement of the impedance presented to the fundamental component, marker 1 in fig. 4.8. Lastly, since the objective is to implement it in a PCB, a short circuit has to be provided in parallel with DC supply at fundamental, 2nd and 3rd harmonics.

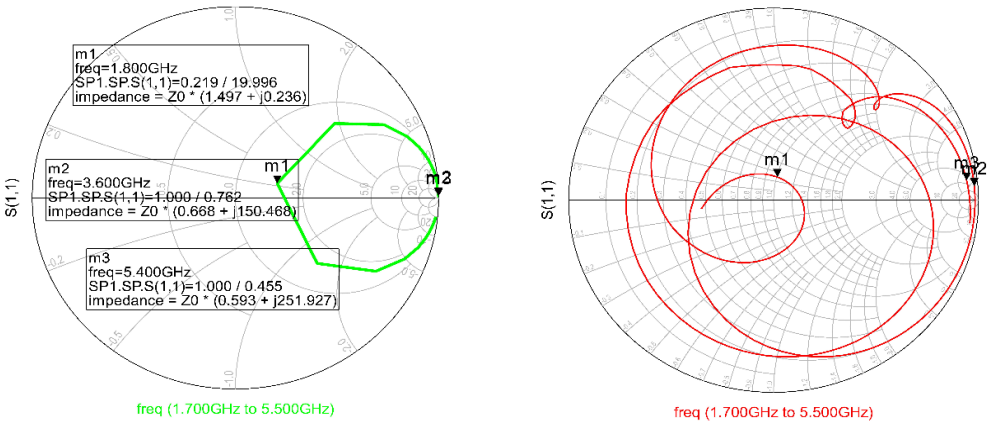

Figure 4.7 – Impedance presented to the extrinsic drain when it is fed through a RF Choke. In the left Smith Chart, the output match is composed only of lumped elements, while the right Smith Chart is composed of microstrip lines.

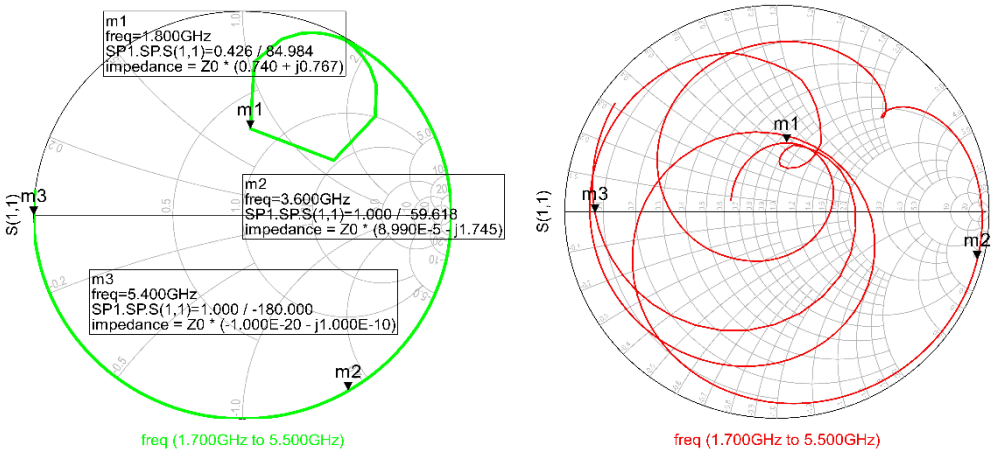

Figure 4.8 - Impedance presented to the extrinsic drain when it is fed through a transmission line. In the left Smith Chart, the output match is composed only of lumped elements, while the right Smith Chart is composed of microstrip lines

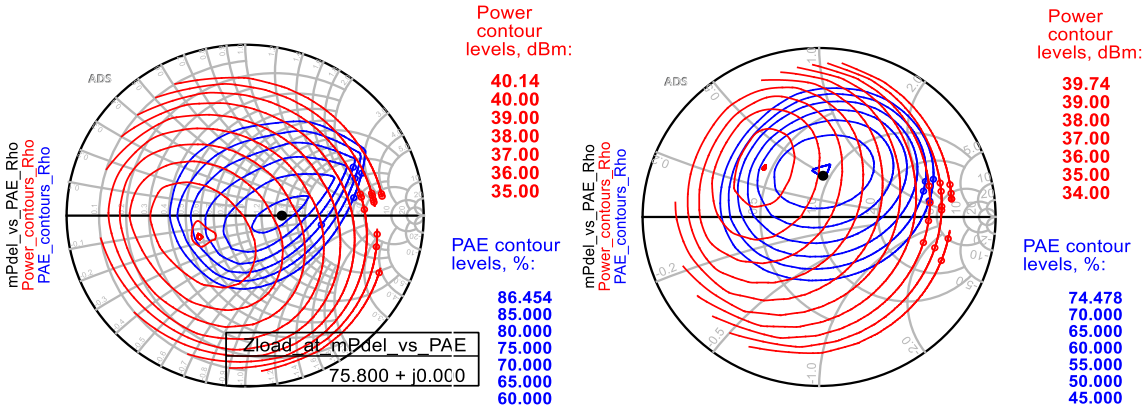

Figure 4.9 – Load Pull contours for the matching network implemented with lumped elements (left plot) and for the matching network implemented with microstrip lines (right plot)

4.5 Chireix with Symmetrical PAs

Having into account the last comments, it is needed to do some modifications at the output match. So, in order to obtain a practicable output match, two radial stubs and one capacitor were introduced in parallel with the DC supply, fig. 4.10. These elements are responsible to ensure that, independently of the impedance presented by the supply voltage, the s-parameters of this network will not change. From fig. 4.12, it can also be seen that the reactive part that has to be presented to the fundamental component was also corrected, and so, a real load is sufficient to achieve the maximum efficiency. Although this load that gives the maximum efficiency is displaced from the center of the Smith Chart, it will not be a problem, because the combiner that will follow this network has the ability to convert the 50 Ohm load to any other resistance value.

Replicating this PA and connecting both with a Chireix Combiner, compensated for a certain angle, it is possible to modulate the load at the output of each PA, fig 4.11. For that purpose, the input power of each PA has to be kept constant, while the phase difference between these signals has to vary, as represented in fig. 4.12 through the orange and green lines. These impedances were plotted in the same Smith Chart of the load pull contours with the purpose to favour its analysis.

Looking carefully to this figure, it is easy to understand that the best situation should have both impedances shifting from the maximum Power to the maximum PAE simultaneously. However, as it was studied in the second Chapter, the impedance presented to each PA is

mandatorily different, being more inductive for one PA and capacitive for the other and so, it is impossible, with these networks, to have this ideal situation.

In figure 4.13, it is shown the impact of each impedance on the respective amplifier. The left plot represents the power that each PA provides to the load, while the right plot represents the respective efficiency, confirming that the second PA is more powerful and efficient than the first one. These results are due to the load that is being presented to them, which in the case of the second PA is closer to the optimal impedance for the maximum PAE and Power delivered.

In the previous chapter, it was explained why these impedance contours are not symmetrical and how they can be shifted in the Smith Chart to improve their power and efficiency. However, as these contours will always behave differently, a new technique was found to overcome this handicap.

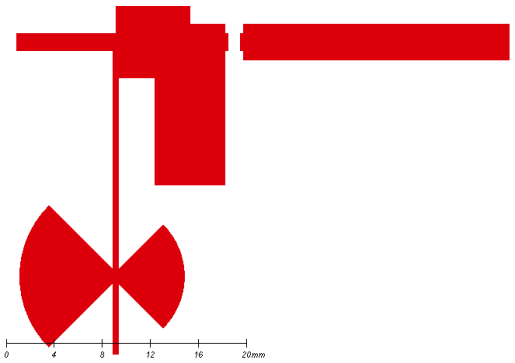

Figure 4.10 – Design of the Output Matching Network

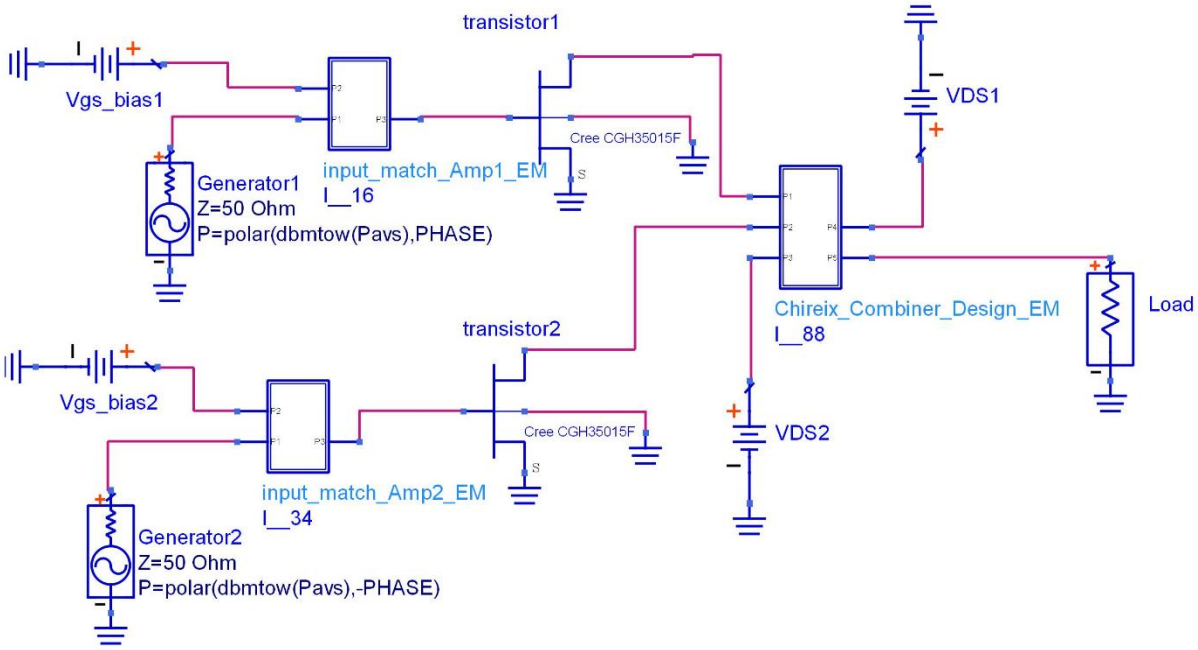

Figure 4.11 – Schematic used to simulate the Chireix Amplifier, in which the output matching networks and combiner are represented by their s-parameters after being simulated with Momentum (Electromagnetic simulator).

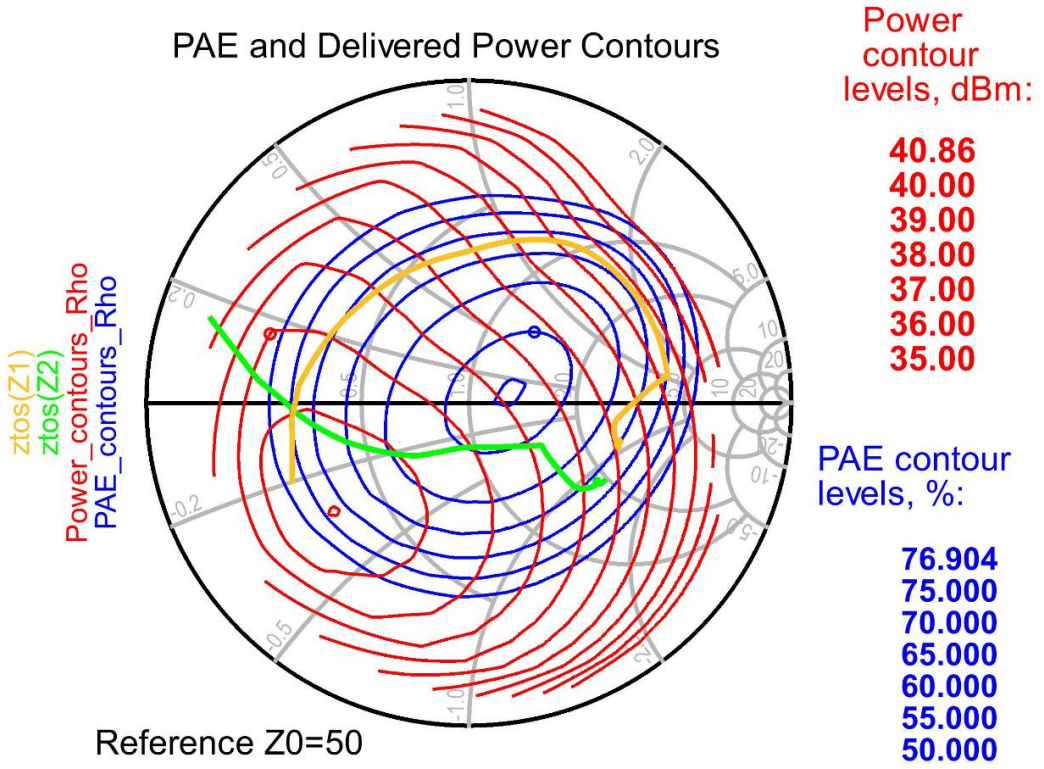

Figure 4.12 – Load Pull Contours for the designed class E PA presenting also the impedance seen by each Amplifier. Green line corresponds to the impedance presented to the second PA, while orange line corresponds to the impedance presented to the first one.

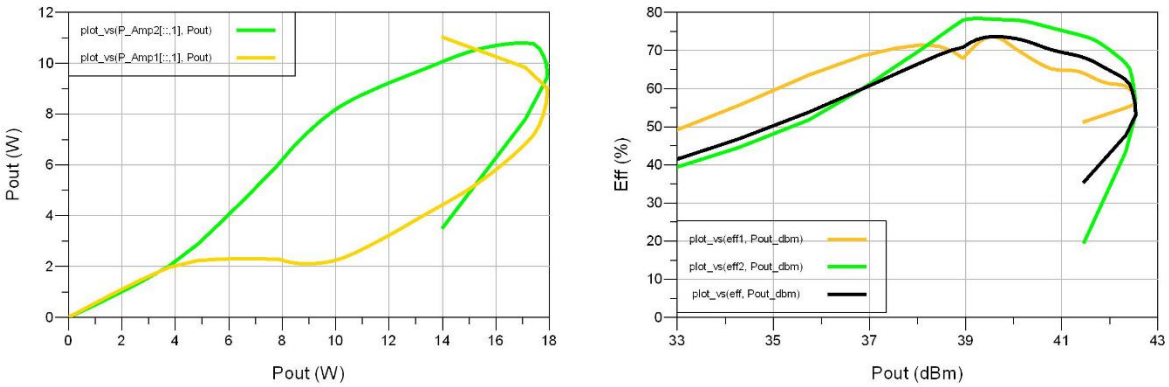

Figure 4.13 – Power delivered by each Amplifier (left plot), and their efficiency (right plot), in which orange and green colors correspond to amplifier 1 and 2, respectively. In the right plot it can also be seen the total drain efficiency of the system, represented with black line.

4.6 Chireix with asymmetrical PAs

Since different impedances will be presented to each PA and the output matching network of each one can be changed, the easy way to improve the efficiency and power is to shift these line impedances through a transmission line, as demonstrated in the previous Chapter. However, as the line impedance of one PA is a bit away from the other, another method will be used. Thus, the output network of PA1 will be redesigned, making it more efficient and powerful for loads more inductive, fig. 4.14 (right plot).

Until now, the asymmetric impedance contours observed in the Smith Chart were caused by the inductive output matching network of both amplifiers. But now, this will be compounded, since both matches are different and the impedance seen by each amplifier is strongly dependent on the signal provided by the other PA, fig. 4.14, green and orange lines.

Despite this setback that weakens the design of the whole system, making it more sensitive to errors that may arise from its implementation, better results were obtained, fig. 4.15. Observing carefully fig. 4.14 (right plot), it must be noticed that this Amplifier cannot reach an efficiency of 70% and although this seems a drawback, the system became more efficient. Another important aspect is that the impedance contour is far from the ideal path

in the Smith Chart, which should start on the load that gives the maximum power, crossing then the load that gives the maximum PAE.

In case of these two situations being improved, i.e., the efficiency of each PA and the path of the line impedances, surely that this amplifier would reach impressive results in terms of PAE, having also margin to increase the maximum output power delivered to the load.

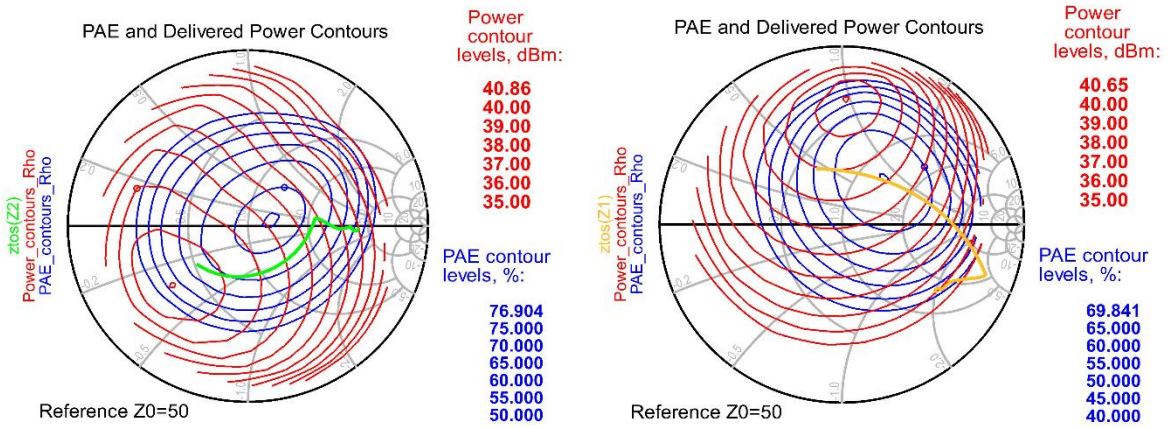

Figure 4.14 – Load pull contours and respective impedance seen by amplifier 2 (left Smith Chart) and amplifier 1 (right Smith Chart)

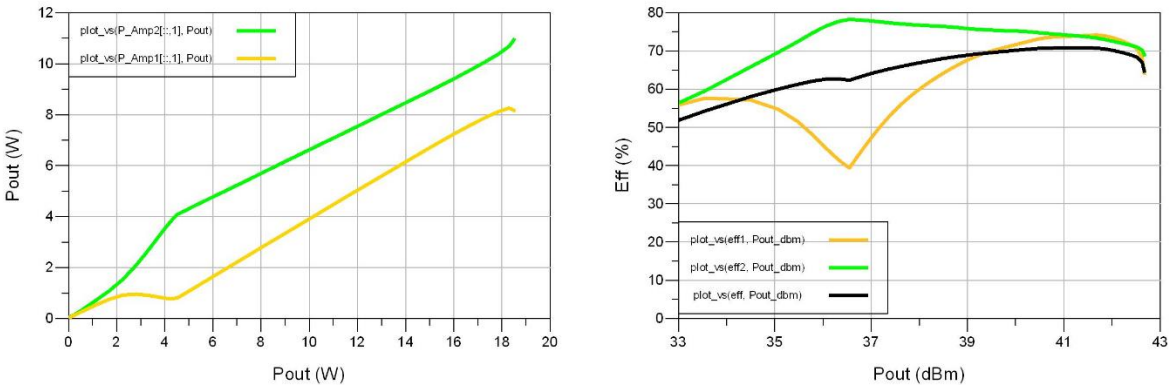

Figure 4.15 - Power delivered by each Amplifier (left plot), and their efficiency (right plot), in which orange and green colors correspond to amplifier 1 and 2, respectively. In the right plot it can also be seen the total drain efficiency of the PAs represented with black line.

4.7 AM – Outphasing with high excursion

Outphasing method assumes a constant input, ideally high, and a different phase for each output power. However, this doesn't make much sense if a low output power is needed. So, to increase the OPBO without wasting too much energy, the input power of each PA has to be reduced [8], making them operating as class B PAs when lower output powers are required. From the simulations done, it was observed that this system provides more power when the signal at both inputs of the amplifiers are almost in phase, and by changing this phase difference between each signal, lower powers can be reached, preserving the high efficiency. Since the power delivered to the load varies, without changing the amplitude of the input of each PA, the gain of each PA has to decrease mandatorily and therefore the PAE also. So, it must be selected a point in which the PAE is not too low and thereafter, reducing the amplitude of each input signal and keeping the phase difference constant, lower powers at the output can be obtained. In other words, the PAs work as class B when lower powers are required and as class E/Outphasing for higher output powers.

Before moving to the signals that control each PA, it is necessary to explain how these signals were determined. Firstly, it was generated a virtual signal, named $Pinput$, then, with this signal, the input power of each PA, $Pavs$, was calculated, through a developed equation, Appendix C, ensuring that this power will not exceed the maximum power that could be provided to each PA. When the $Pinput$ originates the maximum $Pavs$, the process of phase modulation has to start, i.e., the phase difference has to be swept till zero, in which the PAs give the highest power. Having into account that the phase difference has to sweep when the $Pavs$ reaches the maximum allowed power and the phase difference that gives the maximum power is around 0, it is obvious that the initial phase difference has to be a value far from zero, creating margin to sweep it and consequently, originate different powers at the output. This initial phase difference allows to define during how much OPBO the system will be operating as Outphasing. In the ADS simulator, this was done with a logic operator, creating the signals in fig. 4.16 (left plot) exciting then the Chireix Amplifier, resulting on the power and efficiency showed in the right plot. These control signals were calculated in order to change, firstly, the input power of each PA and then, to sweep the phase difference between them. So, the only thing that can be changed is the moment in which the phase modulation starts, through the maximum amplitude of the $Pavs$ signal or through the initial phase difference. However, better results could be achieved in terms of PAE, if a modulation in amplitude and phase were done simultaneously [9].

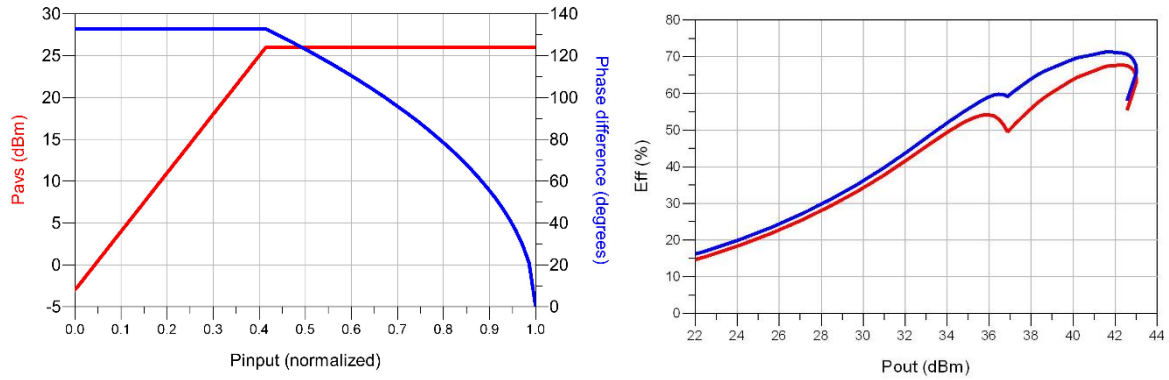

Figure 4.16 – Control signals and system efficiency. Left plot represents the amplitude of the input signals of each PA in dBm and the phase difference between them in degrees. The right plot represents the efficiency (blue line) and PAE (red line) of the system. At 36 dBm of output power, it can be observed the transition between Amplitude Modulation and Phase Modulation.

4.8 Linearization and Improvements

Thus, taking advantage of the ability to set the control signals, the amplitude and phase difference that originate the best PAE for each output power could be found, fig. 4.18 (left plot). Then taking note of these combinations, two differentiable functions, one for each variable, $Pavs$ and phase difference, can be defined. This is exactly what was done (Appendix C), achieving an almost flat gain and possible to be represented by a differentiable function, fig. 4.17. Notice that the gate bias was also changed for a proper value, ensuring a gain at small signal.

It should be highlighted that the gain that is showing in fig. 4.17 is the gain between the output power and the conceptual $Pinput$, and will be called from system gain. In relation to the $Pinput$ signal, it was defined between the range of [-20dBm and 29dBm].

Comparing these new results with the previous ones through the fig. 4.19, it is verified an upgrade in the PAE, reaching almost the limits of this designed Combiner. Moreover, and since the variables that control the input signals can be set independently, the system gain defined previously can be handled to get the shape desired. Despite this being a task for future work, it is shown some simulations with different signals, fig 4.20, in which, the initial phase difference was changed. In the limit, it would be possible to achieve a flat gain if proper functions to generate the control signals were designed, fig. 4.21. This figure was obtained after adjusting the gate bias, sweeping simultaneously the $Pavs$ and the phase difference.

Some published works demonstrated that it is possible to linearize an Outphasing system just by doing pre-distortion to the phase difference [13], [14].

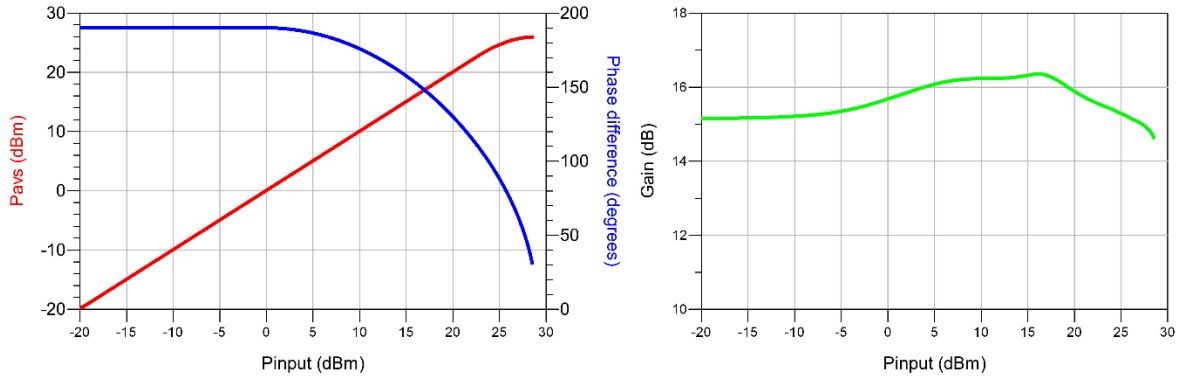

Figure 4.17 - Control signals and gain. In the left plot are represented the controls signals for both PAs, now with the objective to improve the PAE and linearize the gain at the same time, right plot. These input signals were calculated with suited functions, properly developed to this amplifier, having always in mind the objective of be possible to describe the gain by a differentiable function.

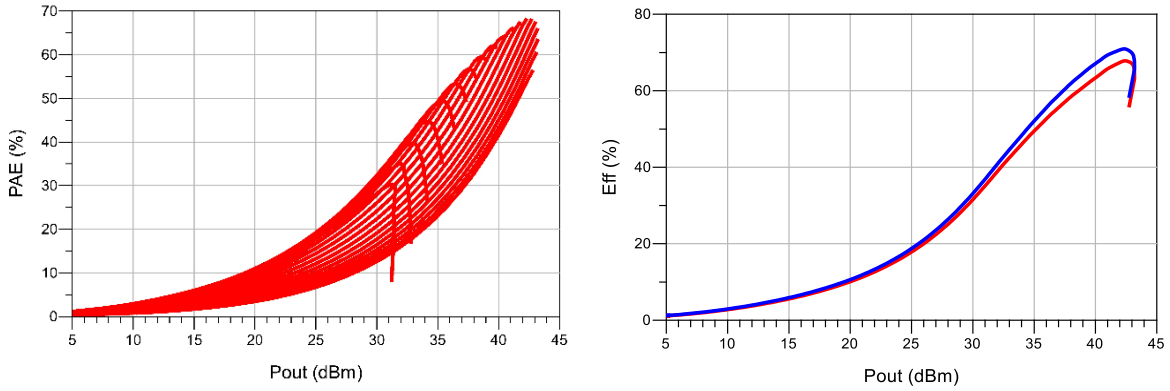

Figure 4.18 – Efficiency for all possible signals. The left plot shows the results obtained when the amplitude and the phase difference of each input signal were swept simultaneously. The right plot shows the result obtained for efficiency (blue line) and PAE (red line) with the control signals represented in fig. 4.17 (left plot).

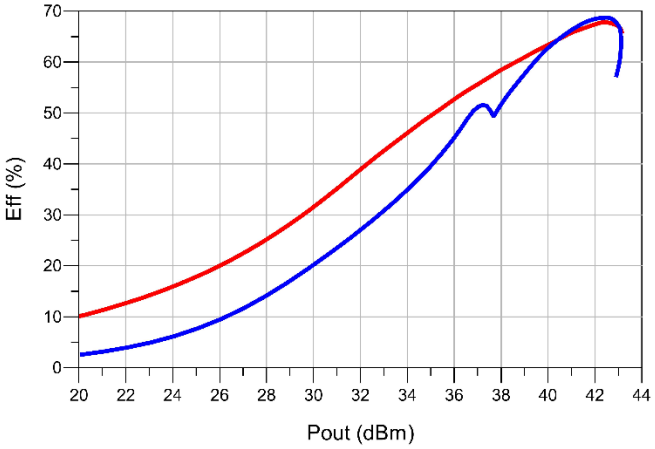

Figure 4.19 – Comparison between PAE when the PA was operating with AM and then Outphasing modulation (blue line) with PAE when the PA was operating with AM and Outphasing modulation simultaneously, called from now on by mix mode (red line). The control signals that gave rise to these PAE values are represented in fig 4.16 and 4.17, respectively.

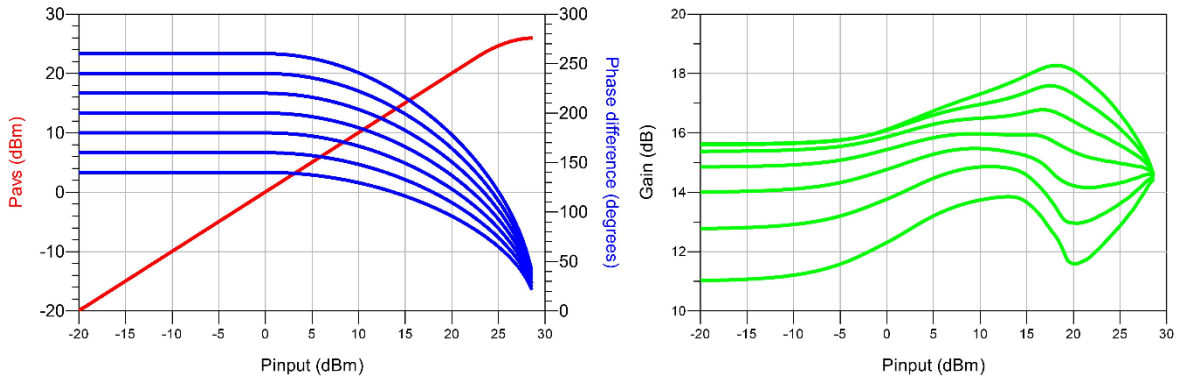

Figure 4.20 – Different control signals and their respective gain. This figure intends to show the effect of changing the control signal that defines the phase difference (left plot) and its respective consequences in the gain shape (right plot).

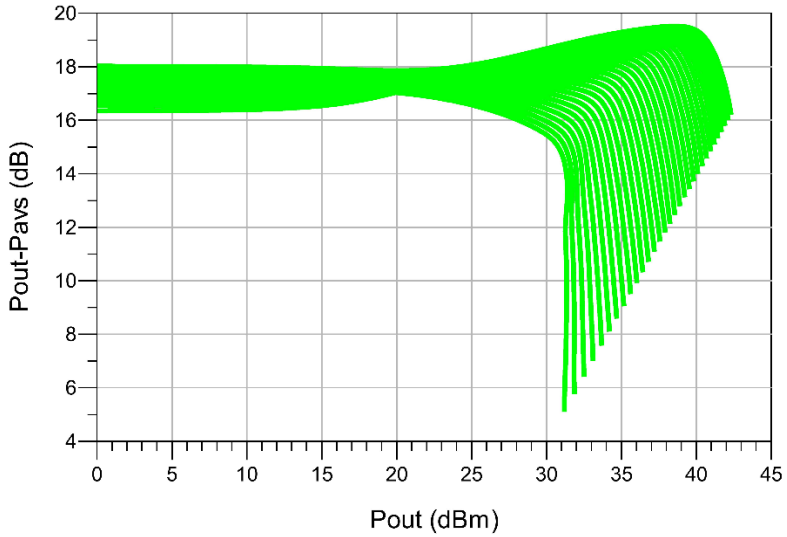

Figure 4.21 - Gain for all possible control signals. This figure shows the impact in the gain when a sweep is done in the input power of each PA simultaneously with the phase difference, proving that for suitable signals it is possible to obtain a gain completely flat.

This Chapter was written with the purpose of offering support to any designer that intends to develop a Chireix Amplifier, highlighting the essential aspects that have to be considered to obtain not only an efficient system but also a linear system. During all this work, some steps were advanced without reaching the ideal conditions. However, for a first design much has been done and surely, if a new design was developed taking into account all these aspects, this new design would be a good candidate to compete with the most efficient PAs built under this configuration, conserving also the linearity of a class B PA, at least when excited with a CW signal.

Regarding to this implemented amplifier, the only way to improve it is by considering that the input of each PA is independent from the other, enabling the control of the amplitude of each PA independently. In that situation, probably, this would be very profitable, since one of the amplifiers is more efficient than the other. However, the only way, for now, to know the best signals to be provided at each PA in that configuration, is by attempts.

To complete the study of all the capabilities provided by this topology it is needed to do a study of the behaviour of this architecture in wideband mode. It is known that handling the controls signals of each PA helps to improve the efficiency for other frequencies [15].

5. Final design and Measured Results

5.1 Layout

In the previous chapter it was shown the input matching network and one of the output matching networks. However, it was proved that, implementing a Chireix Amplifier with different output matches, could result in an improvement of the system. So, the final layout is constituted by two different PAs aggregated with a properly combiner, fig 5.1. Due to the complexity of the whole output matching network, it had to be divided in three parts, two output matching networks and one combiner, in order to compare the simulation realized by ADS software with the electromagnetic simulation done in Momentum software. Since not always the simulations were in agreement, some changes had to be done at the matching networks, approximating both simulations in a long and lengthy process. This process had continuation until the transistors are aligned in x axis and separated with a minimum distance, to place in the PCB the pieces of Teflon. These pieces were used to press each transistor, creating an electric and thermal contact between it and the back plane of the conductor material.

Above the radial stubs, new lines were added to solder some capacitors, which will be responsible to filter lower frequencies preventing the system to oscillate by the DC supply.

The islands around the layout as well as the lines above the stub, were designed to adjust the matching networks. So, in case these matching networks became detuned because of printing imprecisions or in case of the simulations done in simulator are different from the measured results, these islands can be used to tune the circuit.

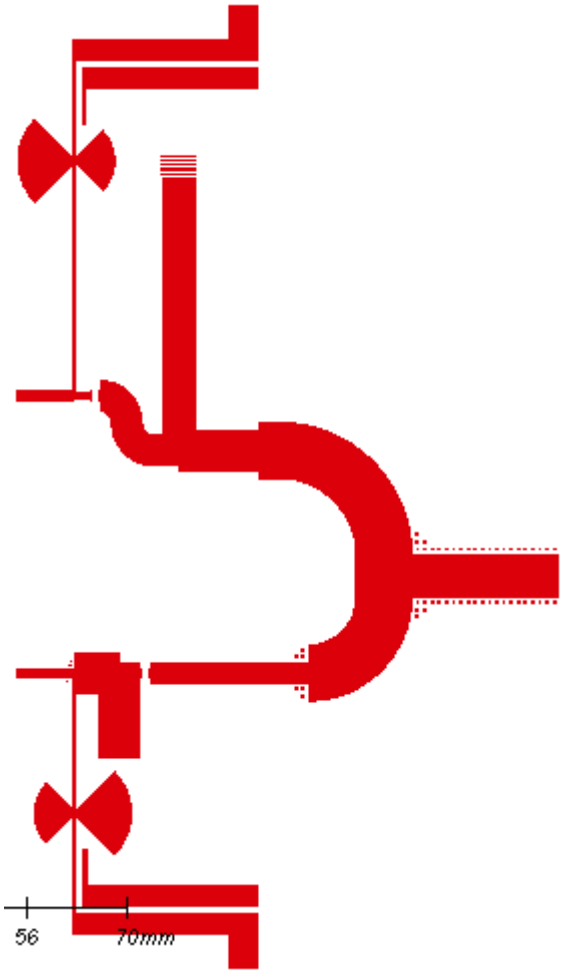

Figure 5.1 – Output matching network layout of the Chireix Amplifier.

After assembling all the matching networks, filing the PCB with ground around the circuit, design some electrical pathways to ensure a ground under the substrate, create some drilling holes to screw the PCB and fix some details, the design was finally printed, using the Rodgers RO4350B as substrate with 0.762 mm of height, fig. 5.2. It was also needed to design a base in aluminium to form the support basis of the PA, enabling to screw not only the PCB but also both transistors and connectors, dissipating at the same time any heat generated by them.

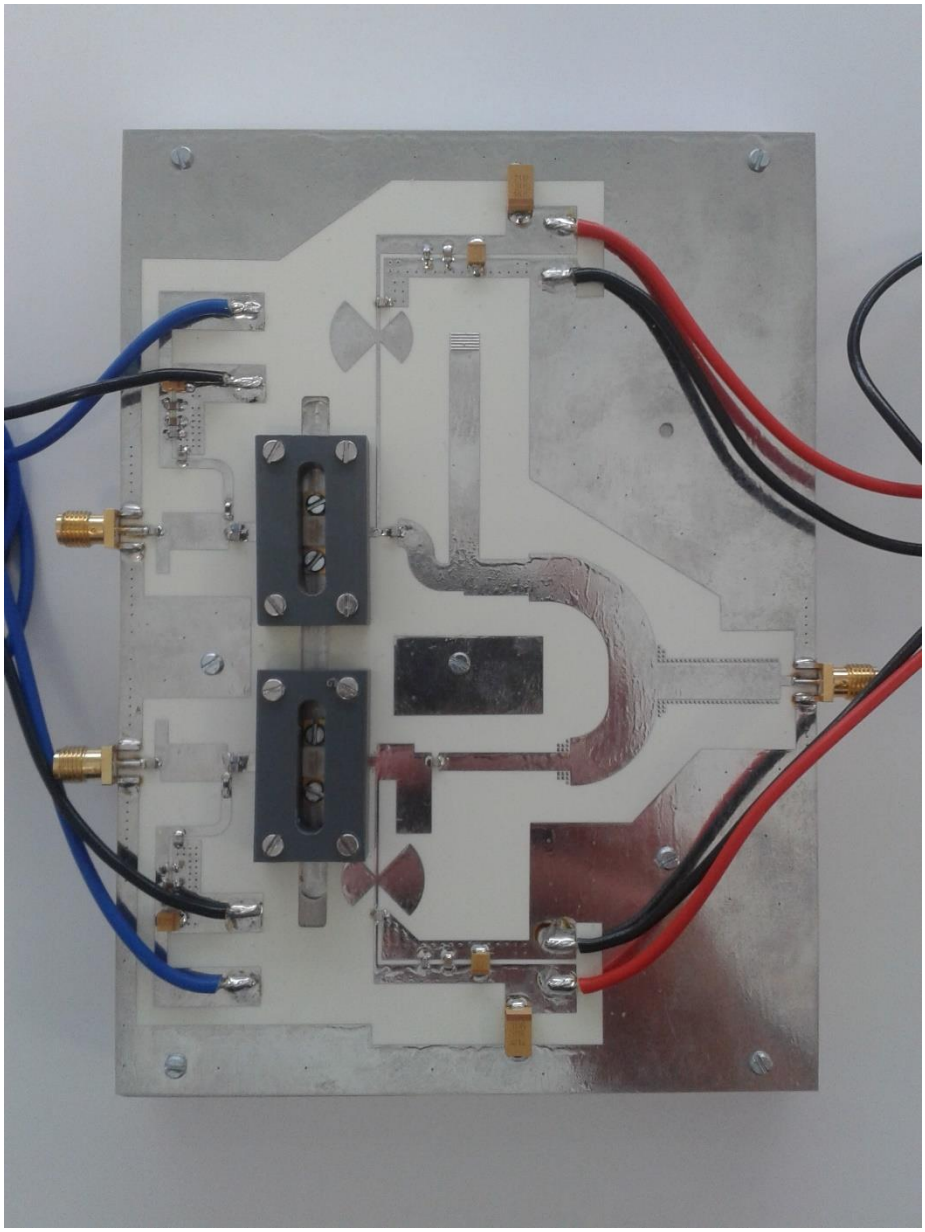

Figure 5.2 – Implemented Chireix Power Amplifier

5.2 Set up mounted to measure the PA

All measurements were made in the RF laboratory of Institute Telecommunications, Aveiro University, and despite this laboratory being incredibly well equipped, it was not found any way to control the phase difference between the signals generated by the VSG. Therefore, and since this is a mandatorily requirement, it had to be used an oscilloscope before the entries of each PA in order to measure this phase difference, adjusting then in the VSG. Although it seems a handicap, it served also to correct any phase deviation during the pre-amplification process in the drivers and correct also any error that could be introduced by the passive elements used behind the oscilloscope, fig. 5.3 and fig. 5.4.

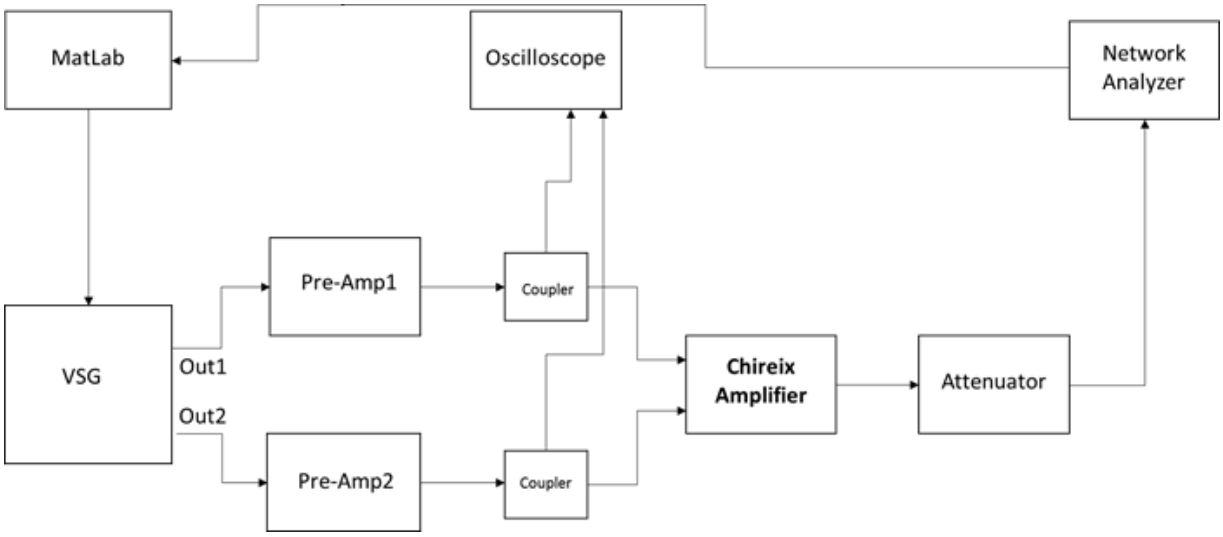

Figure 5.3 – Schematic of the setup built in the lab to test and measure the implemented Chireix Amplifier

Figure 5.4 – Picture of the setup built in the lab to test and measure the implemented Chireix Amplifier

5.3 Measured Results

Before starting to do load modulation with the Outphasing system, both amplifiers were excited individually with a CW signal at 1.8GHz, measuring then their output power through the Vetor Network Analyser. This test was done with the intention to find any oscillation and to evaluate the gain of both PAs. Thereafter, both PAs were excited with the same signal simultaneously, to test their performance when operating in parallel, starting also with small signal and going then to large signal carefully, fig. 5.5 and 5.6. Comparing the simulated results with the measured ones, it can be verified a loss in the gain of 0.5dB and also a loss in the efficiency of 5%. The shape of the gain is also a bit different but since the difference is verified at large signal, it can be caused by trapping effects, most known by soft compression [16]. Note that the gain presented in the next 4 figures, is the signal gain, i.e., the output power less the power available at each PA input. To confirm that the system was

in accordance with the results obtained in simulation, the phase difference was changed to 130 degrees. Fortunately, the results observed were again closer to the simulated ones, with exception to the maximum efficiency that was a little below than the expected. However, this difference was reduced afterwards to change the phase difference in simulation to 152 degrees, fig. 5.7 and 5.8. Comparing again the gain measured with the gain simulated, it can be seen, newly, a different shape, but now, this shape cannot be only due to trapping effects. Analysing the efficiency plot with more detail, it can be verified that at lower output power, the measured results present more efficiency, and so, it can be concluded that the loads that are being presented to each PA are different from the simulation. Reason why this system becomes more efficient and with different shape for the gain between fig. 5.7 and 5.8.

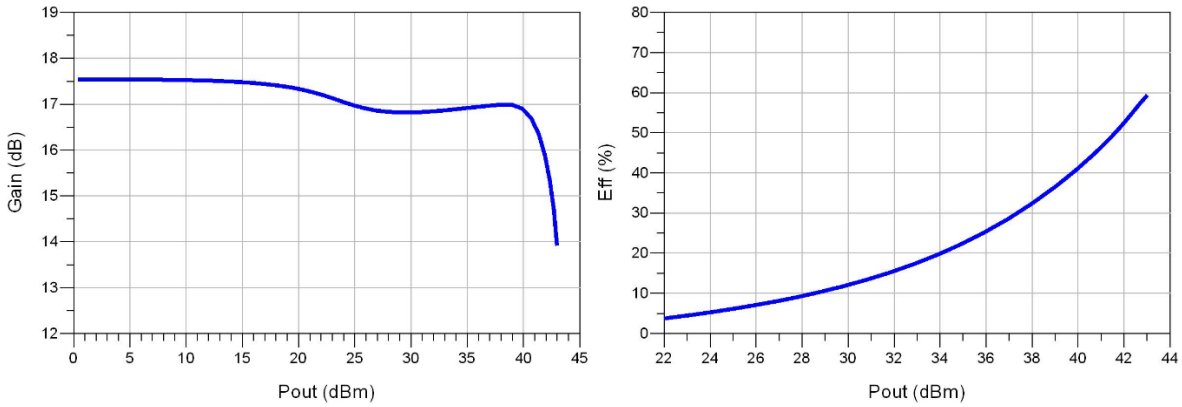

Figure 5.5 – Simulated results for both inputs in phase varying only their amplitude.

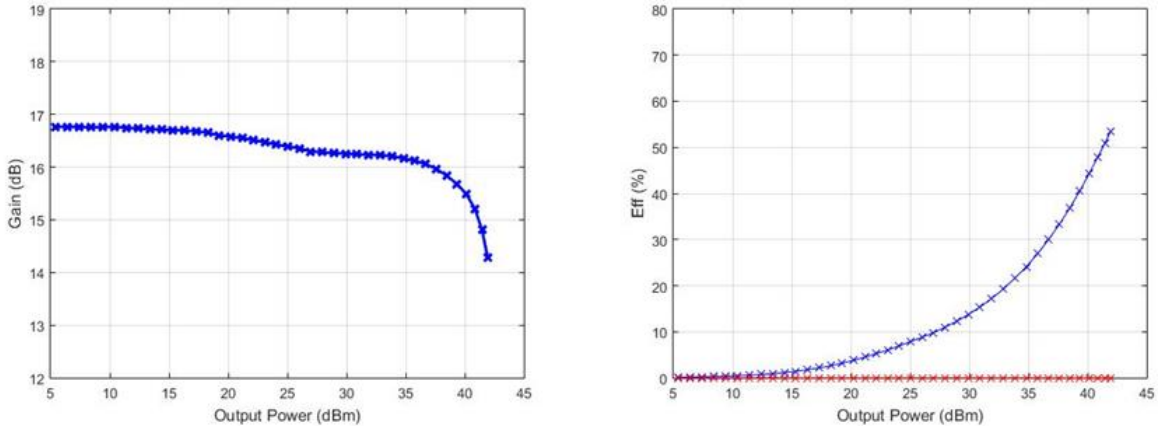

Figure 5.6 - Measured results when both inputs are in phase varying only their amplitude

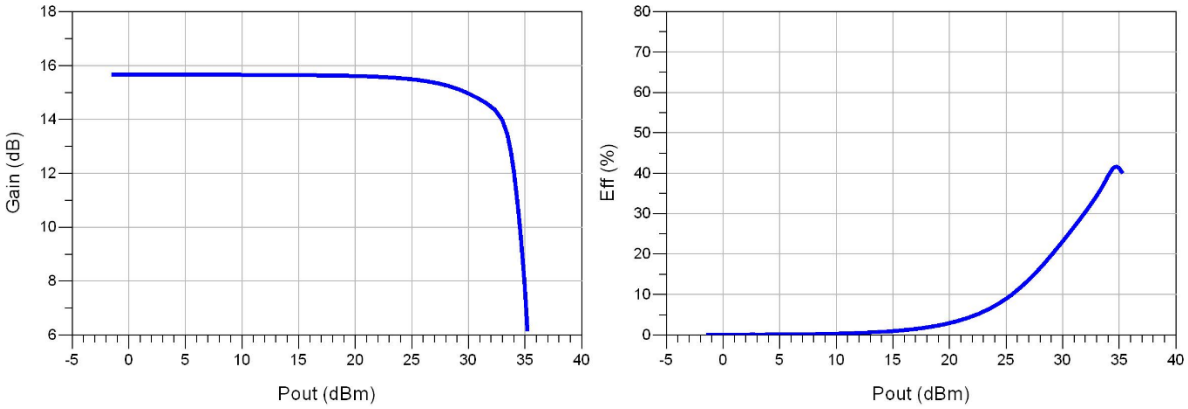

Figure 5.7 - Simulated results when the inputs have 152º of relative phase shift varying only their amplitude.

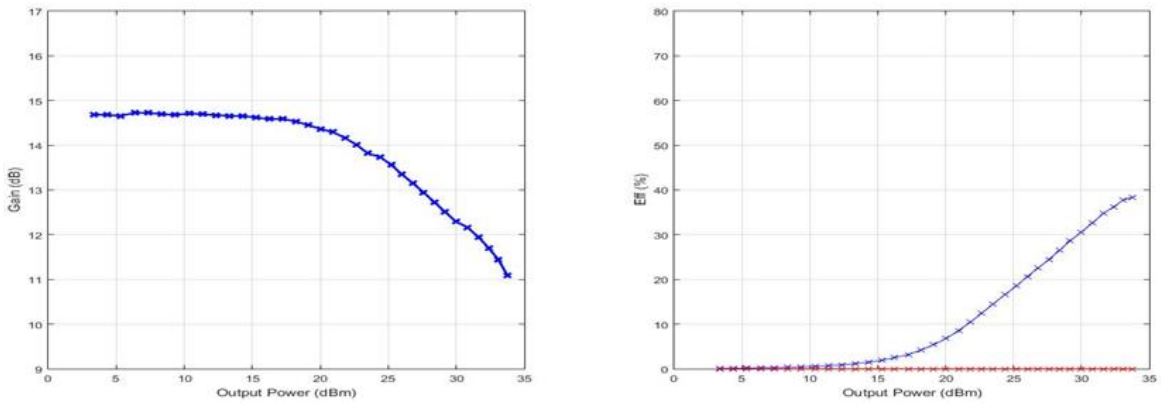

Figure 5.8 - Measured results when the inputs have 130º of relative phase-shift varying only their amplitude.

These first steps were very important to detect any anomaly in the design, verify the setup mounted and the code running on Matlab in real time, which had enabled the remote control over all devices.

After that, with the objective to prove the Outphasing concept, a $Pinput$ vector was generated and the signals to be sent to each PA, were calculated. For that, the function created in Matlab was used again, but this time, with the aim to send them to the VSG.

The first control signal generated was the same showed in fig. 4.16 (previous chapter) resulting in the values represented in fig. 5.9. These results can be compared with the results obtained in the simulation, red line, after being added an offset of 8 degrees to the phase difference, matching the point of transition between the AM and Outphasing signal in terms of output power. From the left plot, it can be seen a drop in the PAE, being then increased for OPBO higher than 9dB, yet, its shape is not much different from the simulated one.

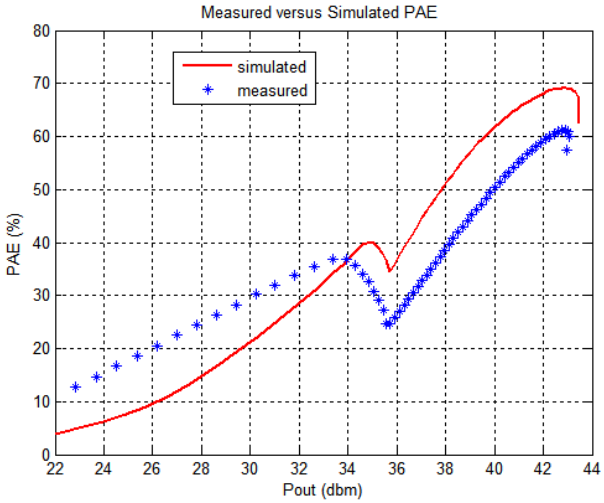

Figure 5.9 – Simulated versus measured PAE for system operating first as AM and then as Outphasing system.

Since the maximum PAE measured is a bit far from the simulated one and knowing that the model used to characterize the transistor describes relatively well its behaviour, it can be thought that the simulator was not capable to predict with precision the s-parameters of the designed output matching networks. This belief can be sustained by the fact that during the simulation, some deviations were found between the ADS simulator and the Momentum tool.

Going further and taking advantage of being possible to manipulate the input signals of each PA, the same control signals of fig. 4.17 were used, mixing the concept of Outphasing with Amplitude Modulation, having direct impact in the PAE, fig 5.10. Although the measured results for PAE using AM followed by Outphasing modulation can be changed, they will never reach the results obtained using the mix mode operation, at least for this designed PA. Since this plot represents the PAE for two modes of operation, it is therefore appropriate to present a measurement of a class B PA and a Doherty PA with the same transistors, making possible a comparison between all them.

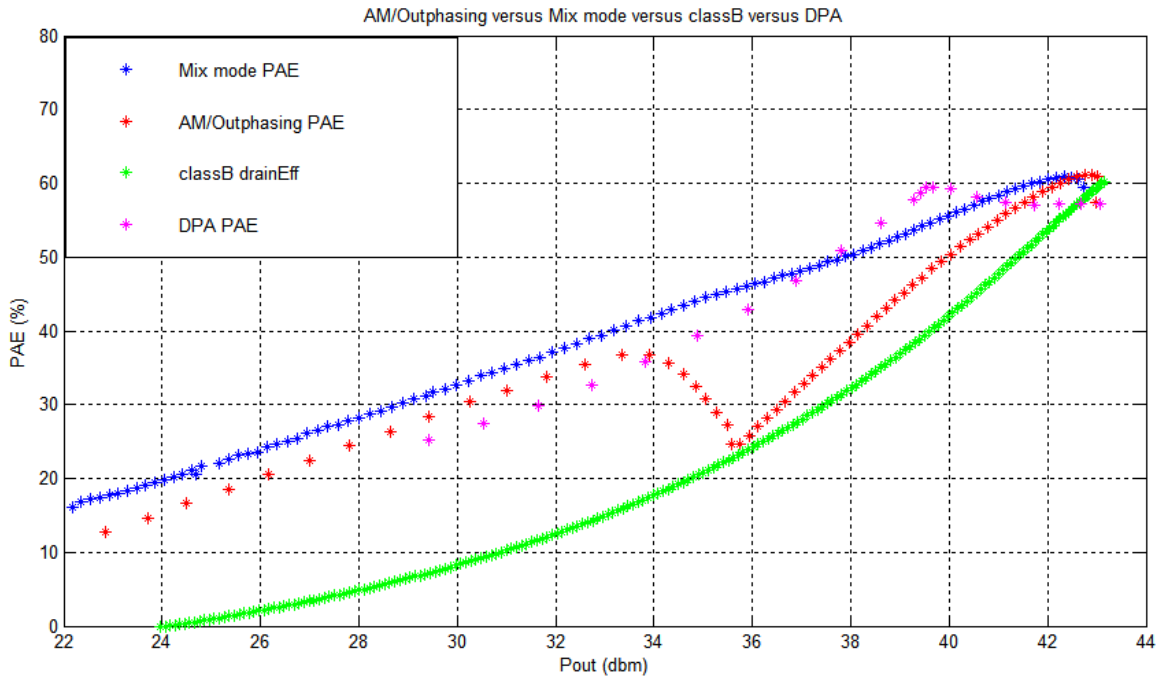

Figure 5.10 – Measured results for four different topologies. Mix mode means that the control signals were modulated in amplitude and phase simultaneously. For AM/Outphasing means that the signal was modulated first in amplitude and then as an Outphasing system. DPA stands for Doherty Power Amplifier and the last one is a class B PA. DPA and class B PA correspond at two works developed by two students in Institute of Telecommunications in Aveiro University. Their output power and efficiency were normalized to the results obtained in this work.

Since again, comparing the results simulated with those obtained in the laboratory, under the same conditions in terms of control signals, it verifies a drop in the PAE for higher output powers and an improvement for lower output powers, fig 5.11. Although this result is a bit lower than the result obtained in simulation, it presents a PAE of almost 40% at 10dB PAPR, keeping a gain almost flat and possible to be handled.

This method of mixing the input signal with AM and Outphasing modulation simultaneously, allowed to approximate the PAE with the drain efficiency, fig. 5.12 (right plot).

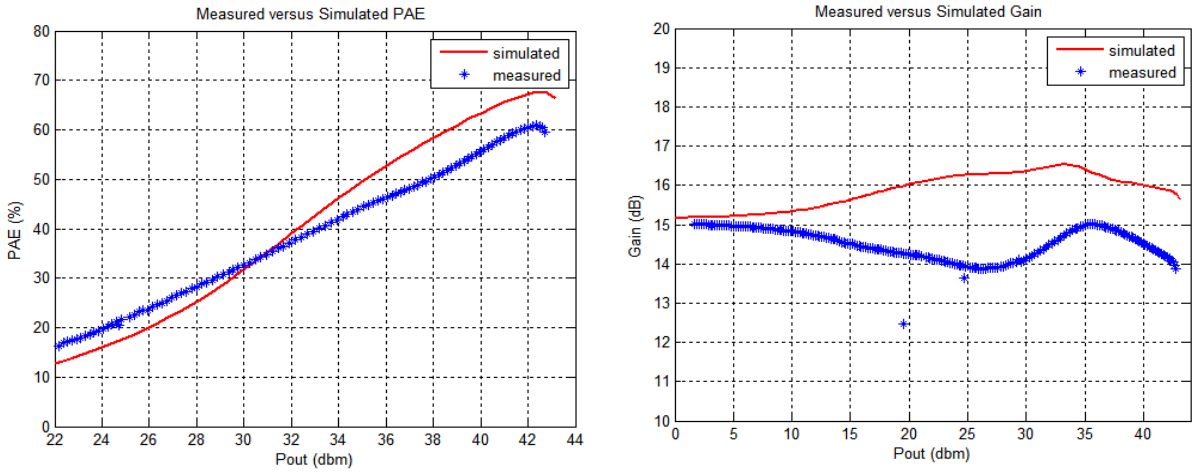

Figure 5.11 - Simulated versus measured PAE for system operating as AM and Outphasing simultaneously.

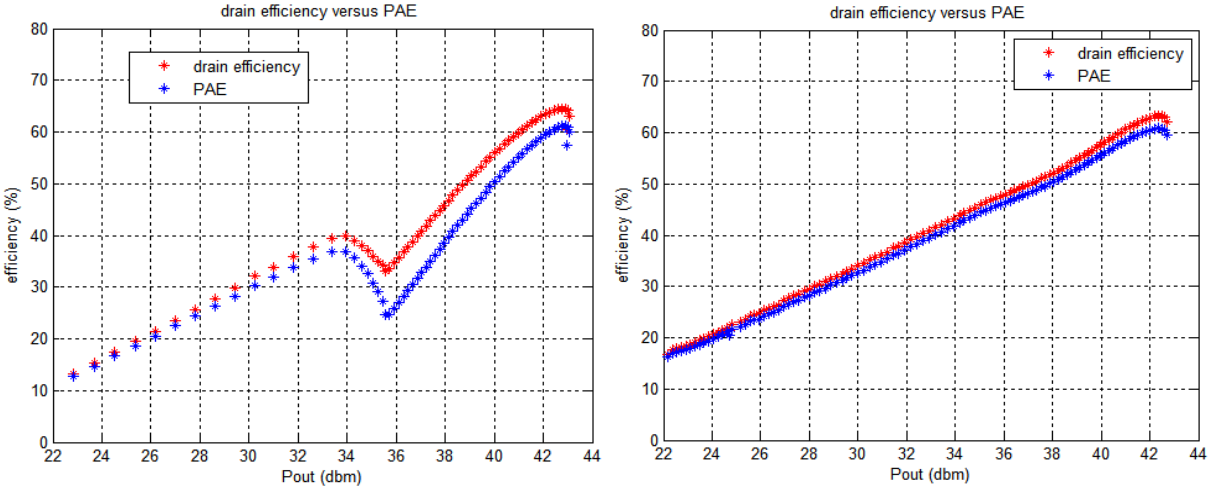

Figure 5.12 – Measured results for drain efficiency and PAE when excited with AM and then Outphasing signals (left plot) and in mix mode (right plot).

5.4 Bandwidth

This system was not designed to be a broadband Amplifier, yet, for being tested with a modulated signal, it cannot be tuned to just one frequency. So, a new CW static signal was generated in order to measure its response at different frequencies, fig 5.13. In this figure are represented the frequencies where it has an acceptable behaviour, and from that, it can be concluded that this signal presents a similar PAE in a bandwidth lower than 10MHz, centred in 1805MHz. In the same figure (right plot), it can also be observed the system gain from the $Pinput$ to the output for different frequencies. Those verified high deviations may

become a drawback to this particular designed system, since it can be a source to the nonlinearities if it operates with a signal having a considerable bandwidth.

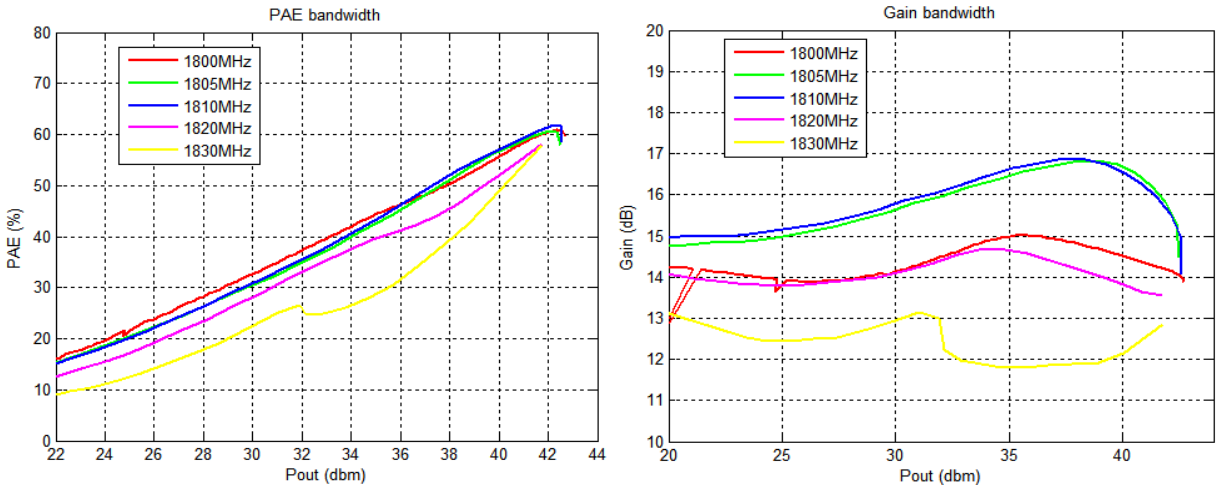

Figure 5.13 – Measured PAE and Gain for different frequencies

5.5 Modulated Signal

Until now, all measurements were done with a CW static signal, meaning that the initial condition for each measurement was always the same. However, the signals used in telecommunications systems, are fast and continuous, i.e., the system can be operating at the maximum power in one moment and microseconds after at the minimum power level. Besides that, those signals have a certain bandwidth, and so, the baseband signal will present a frequency much lower than the carrier frequency, facing different conditions in the system. It is known that the PAs and in particular GaN HEMT transistors are strongly dependent on memory effects [16], so the only way to ensure that this architecture and in particular this PA are prepared to operate with the signals used nowadays, in telecommunications systems, is to excite it with a real signal.

Therefore, a signal was built under the LTE standard with a PAPR of 9.4dB, 5MHz of bandwidth and a carrier frequency of 1.8GHz, fig 5.14. However, before sending this signal for each PA it was needed to calculate the amplitude and phase that allow a full recovery of the input signal as was explained in the previous Chapter, generating the control signals represented in fig. 5.15. Since the transfer function that originates those control signals is nonlinear, a first distortion of the spectrum is verified on this stage, fig. 5.16. Notice that, one is more distorted than the other, due to the fact that one of the signals kept its phase

while the other signal has its phase adjusted for a proper value, ensuring the difference phase needed between both signals.

After the signals being applied to the system, through the VSG, the AM/AM and AM/PM conversion for the input to the output were measured, fig. 5.17 and fig. 5.18. In the first case, a completely different gain of the CW measurements can be observed, presenting a shape of a class C Amplifier, and although this seems awkward, this feature is well known by the PA designers and is associated to trapping effects [23].

Regarding to the AM/PM feature, it can be seen a high distortion at the maximum output power, and since the power delivered is not raising, the $Pinput$ signal has to be reduced.

A few lines ago, it was said that the signals sent to each PA had already the spectrum distorted, yet, if the both PAs had the same gain and their phase were preserved, making the system linear, these distorted signals would be cancelled in the system output. However, this was not the case, and so, the adjacent channels were high distorted, fig. 5.19. Since the gain was already nonlinear when the system was excited with CW signal, it cannot be inferred if the spectrum regrowth is weak by the nonlinearities inherent to the design or if it is a direct consequence from the memory effects of the transistors. Thus, and with the aim to conclude the discussion on the main sources of nonlinearities, a simulation with 2 tones for each amplifier input was made in ADS simulator [25]. In order to ensure the same process of modulation done in the laboratory, it was needed to generate a baseband signal in Matlab, calculating then, the control signals to be provided at each PA input. After that, those values were transferred to ADS, being generated with a source power and then modulated with RF signal (2 tones). This method allowed to overcome the density of information that composes the LTE signal by a simple signal that can be decomposed with a small number of frequencies, enabling the simulation of the Chireix PA when excited with a baseband signal. The signal used in baseband to simulate it, was a cosine, which has a PAPR of 3dB, far from the 9.4dB of the LTE signal generated and with bandwidth of only of 1MHz. To make matters worse, the PA matches used in this simulation were not simulated in Momentum, and because of that it was verified an increase of power in the system output, fig. 5.20 (left plot). All these problems could be solved if a proper signal was developed to present a PAPR of 9.4dB and if the PA matching networks were simulated in momentum for frequencies near the baseband. A last problem can remain in the s-parameters files of the components used. Nevertheless, the main difference between the simulation and the measured results lies on the trapping effects introduced by the GaN HEMT, which are not represented on the model used to simulate the system. So, since these effects are causing a completely different shape of the gain, it can be conclude that besides the Chireix gain

simulated with 2 tones is almost flat, the designed system presents some distortion in the output, unlike that was expected, fig. 5.21.

However, from fig. 5.20, it can be observed that other kind of memory effects are causing a hysteresis on the system. Since these memory effects are being observable at the baseband frequency, it means that they have origin in long time constants. In fact, there are some possible sources, yet, since the path to the output of one PA is greater than the other and the gain returns by above when the envelope is falling, it might be speculated that this verified hysteresis can be due to the path imbalance of both PAs, being then reduced for signals with lower bandwidth, fig. 5.22. Still and despite this explanation be reasonable, it was not validated, and so, a more carefully analysis should be done.

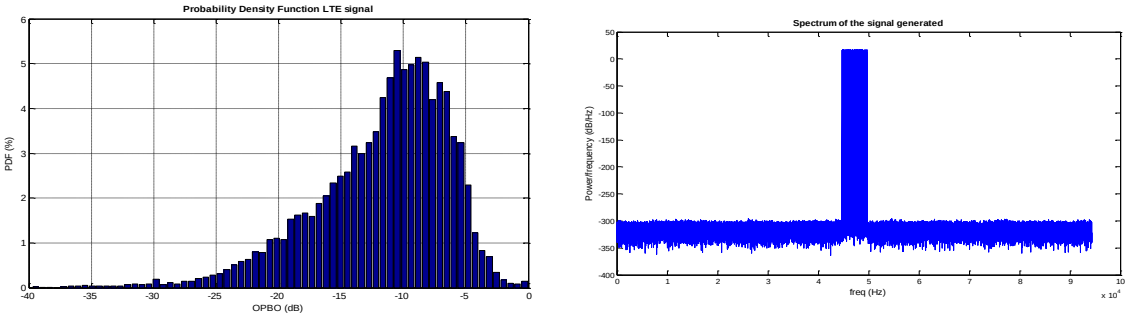

Figure 5.14 – PDF and Spectrum of the LTE signal generated with a PAPR of 9.4dB and a 5 MHz of bandwidth.

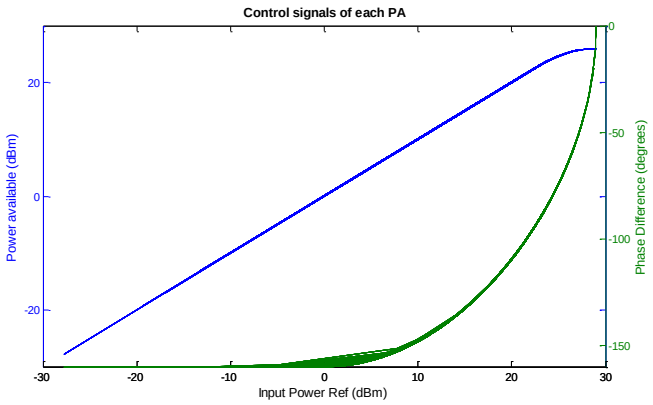

Figure 5.15 – Control signals originated by modulated signal.

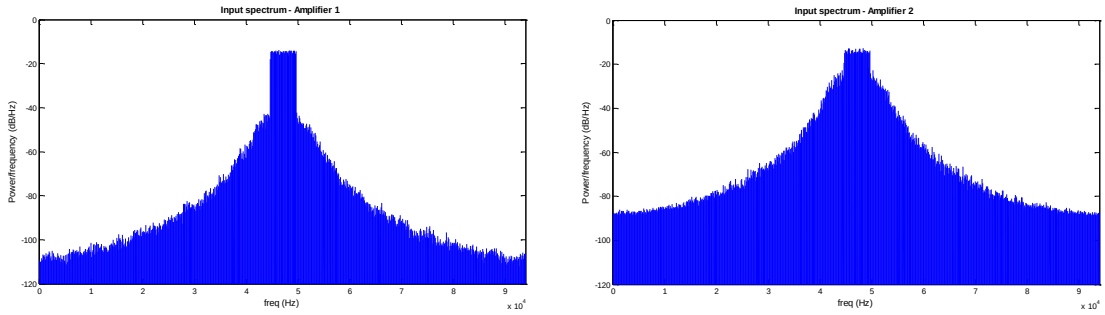

Figure 5.16 – Spectrum of each PA input. Left plot corresponds to the signal that preserved its phase.

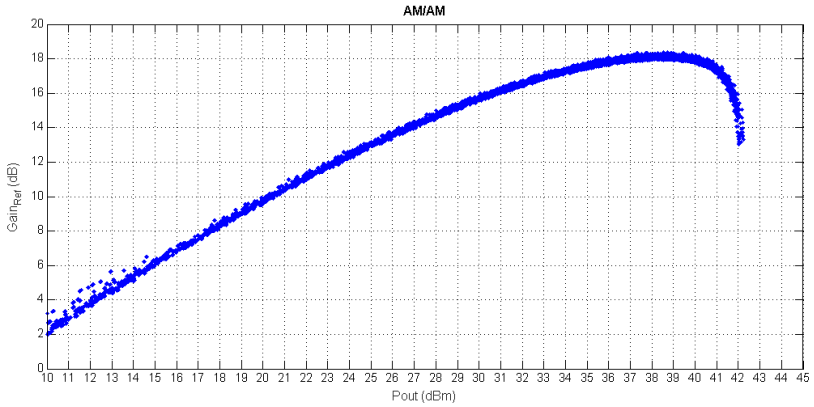

Figure 5.17 – AM/AM distortion measured for the modulated signal.

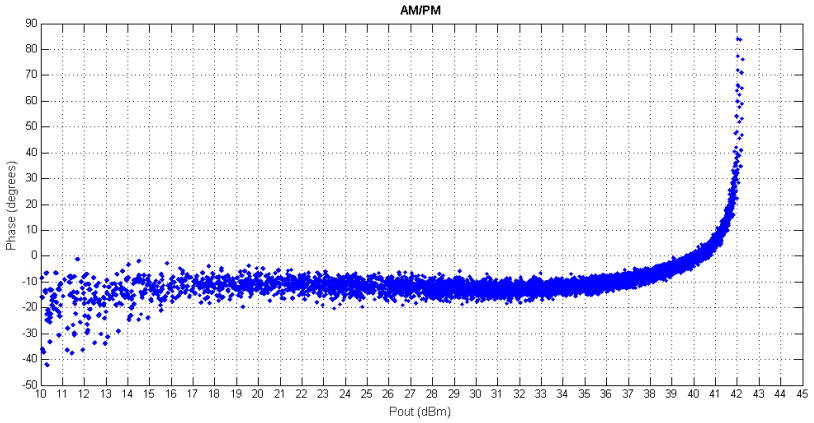

Figure 5.18 – AM/PM distortion measured for the modulated signal.

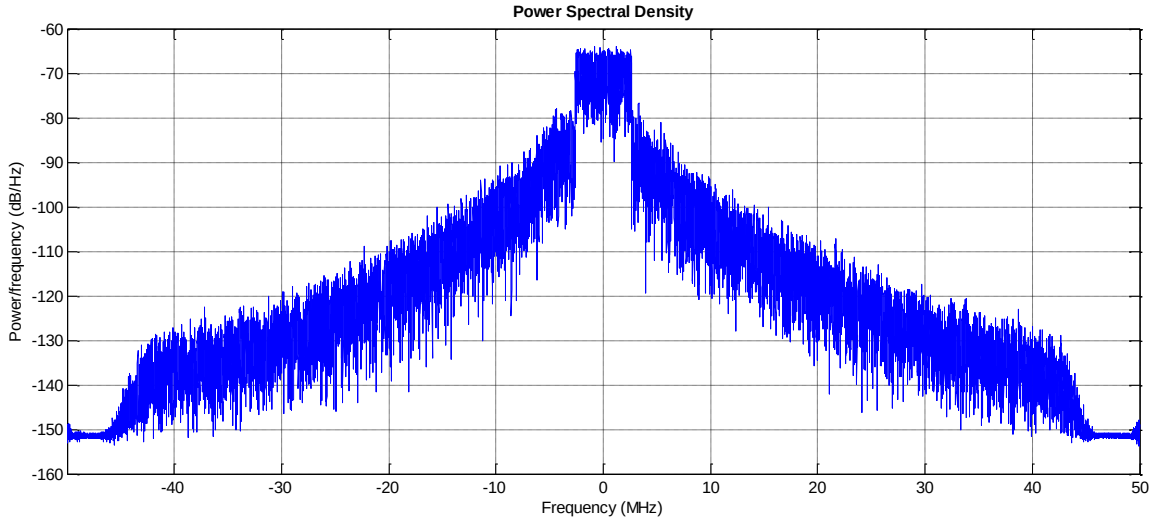

Figure 5.19 – Measured System Output Spectrum for the modulated signal.

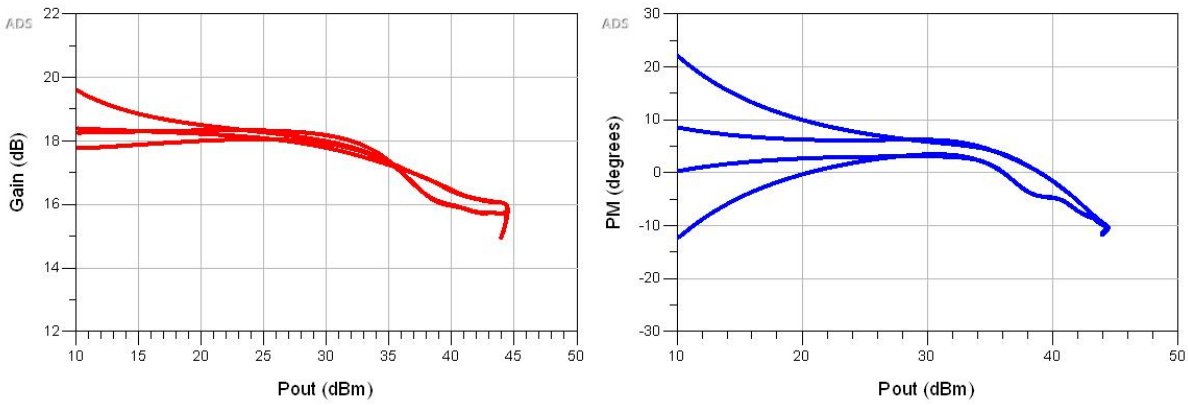

Figure 5.20 – AM/AM and AM/PM simulated with 2 tones separated by 1MHz.

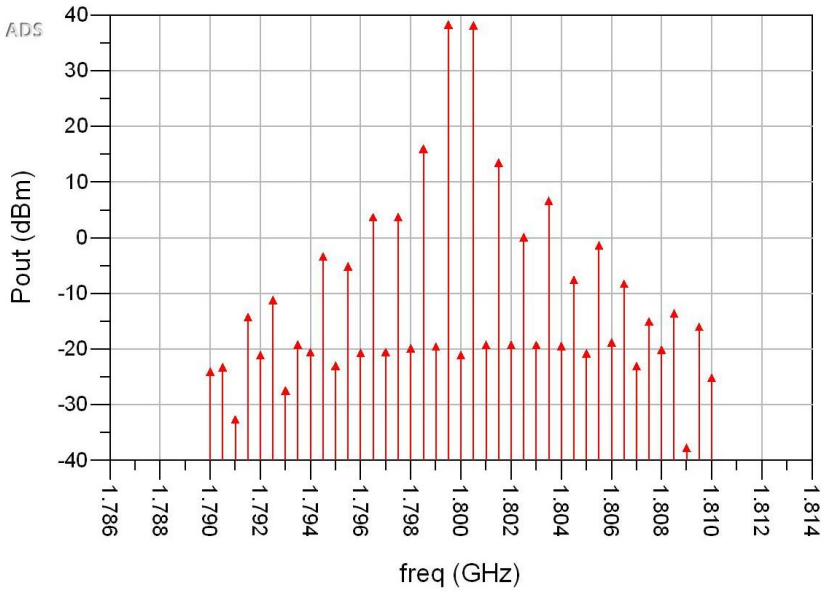

Figure 5.21 – System Output Spectrum performed by ADS simulator with 2 tones at each PA input with 20th order of the envelope and with a bandwidth of 1MHz.

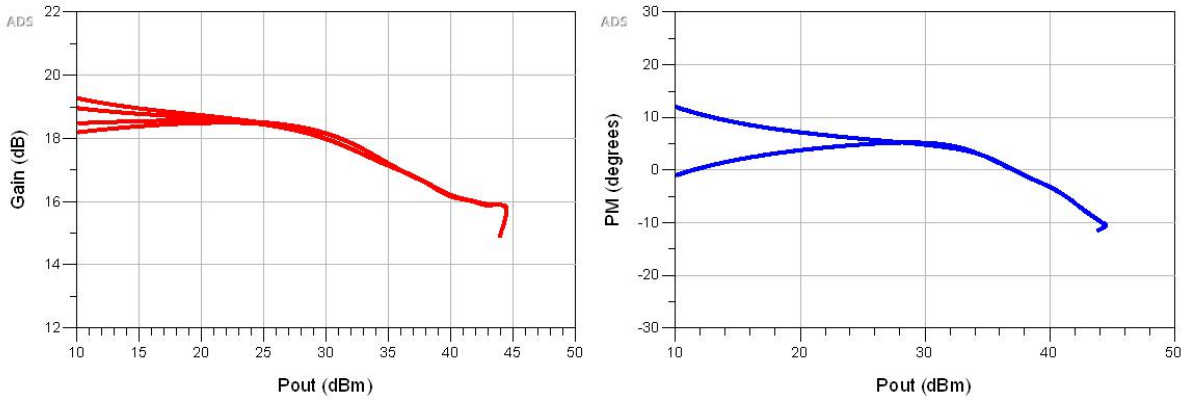

Figure 5.22 - AM/AM and AM/PM simulated with 2 tones separated by 10KHz.

6. Conclusion

The objective of this dissertation was to implement an Outphasing system with a Chireix Combiner. Its aim was to understand the load modulation caused by the combination of two signals with different phases, as well as the transfer function from the input to the output. Regarding the first objective, it can be said that the theory behind this concept, studied in Chapter 2, is consistent with practice, as demonstrated in Chapter 3. However, the idea that both PAs are always operating with the maximum efficiency is misleading, as was proved with the Load Pull Contours and the load modulation. Moreover, it was seen that, PAs have to be carefully designed, looking always to the trajectory of the load modulation in the Smith Chart. In terms of the system linearity, it was concluded that the control signals of each PA can be properly suited to make the system linear as possible, giving up only from the high efficiency. During this dissertation, it was highlighted the main characteristics that a designer should worry about in order to achieve the best performance in terms of PAE or in terms of linearity, and although some steps were advanced without reaching the ideal conditions, the final results were shown to be very promising.

Although the objective of this work was just to study the behaviour and linearity of an Outphasing system, our will and enthusiasm, led us to explore a bit more the behaviour of this system in the presence of asymmetric PAs and under the operation of mix mode signal. Unfortunately, some inconsistency between the simulation results and the results measured in the laboratory was observed.

Nevertheless, we are convinced that, if the maximum efficiency of each PA was improved by changing the impedance presented to each harmonic, and if the output match of the first combiner was adjusted, probably, the results that would be measured from this system would be closer to the best results reported until now. Yet, it would be needed to investigate the coherency of the transistor model and the electromagnetic simulations of the matching networks with the results observed in practice.

For now, the PAE of those works, is being reported between values of 40% and 50% for a modulated signal with 5MHz of bandwidth and a PAPR of 9.6dB [9, 17-19], against the 34% verified in this work, being overcome only by the 3-way Doherty Amplifier [21] or the 4-way Outphasing [20]. So, it will be not surprisingly, if, in a few years, some designs of PAs with Doherty and Outphasing configuration operating together as a unique system begin to appear in the market.

For now, and following-up this work, the main task that has to be done, is to understand the nonlinearity sources of the system, to then linearize it with the aim to meet the requirements of the market, enabling the use of this architecture.

The last results presented in the last chapter, with respect to the simulation done in ADS with 2 tones, can be considered as an extra of this work and a bridge to the future work, highlighting the problems associated to distortion when operating with large bandwidth and the high contamination of the output spectrum, which seems to be a direct consequence of this architecture.

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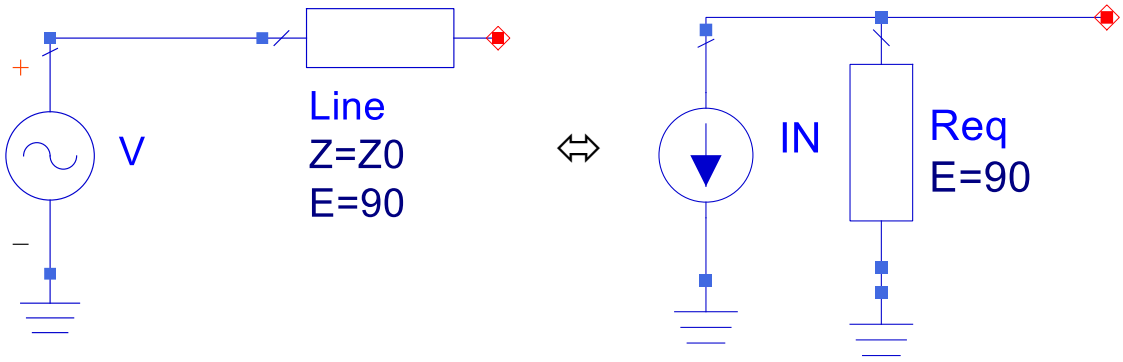
Appendix A

Transmission Line



Calculating Norton Equivalent

Incident Wave: $V_i e^{-j\beta x}$
Reflected Wave: $V_r e^{j\beta x}$

Short Circuit:

$$\begin{cases} V(0) = V_i + V_r = Ve^{j\theta} \\ V(l) = V_i e^{-j\beta l} + V_r e^{j\beta l} = 0 <=> V_i e^{-j\beta l} = -V_r e^{j\beta l} \end{cases}$$

$$<=> \begin{cases} -V_r e^{2j\beta l} + V_r = Ve^{j\theta} \\ V_i = -V_r e^{2j\beta l} \end{cases}, \beta l = \frac{\pi}{2}$$

$$<=> \begin{cases} V_r = \frac{Ve^{j\theta}}{2} \\ V_i = \frac{Ve^{j\theta}}{2} \end{cases}$$

$$I_N = \frac{V_i e^{-j\beta l} - V_r e^{j\beta l}}{Z_0} = \frac{\frac{V}{2} e^{j\theta} e^{-j(\frac{\pi}{2})} - \frac{V}{2} e^{j\theta} e^{j\frac{\pi}{2}}}{Z_0} = -\frac{jVe^{j\theta}}{Z_0}$$

$R_{eq} = \frac{Z_0^2}{0} = \infty$, from the $\frac{\lambda}{4}$ impedance inverter

Appendix B

Proof of the equations presented during the dissertation

$$Acos(wt) = kcos(wt + \theta) + Kcos(wt - \theta) \quad (2.1)$$

$$= kcos(wt)\cos(\theta) - k\sin(wt)\sin(\theta) + kcos(wt)\cos(\theta) + ksin(wt)\sin(\theta)$$

$$= 2Kcos(\theta)\cos(wt)$$

$$\Leftrightarrow \theta = \cos^{-1}\left(\frac{A}{2K}\right) \quad (2.2)$$

$$Z_1 = \frac{V_1}{I_0} = \frac{Ke^{j\theta}}{\frac{j2Ksin(\theta)}{R_L}} = \frac{1}{2}R_L(1 - j * cot(\theta)) \quad (2.6)$$

$$Z_2 = \frac{V_2}{I_0} = \frac{Ke^{-j\theta}}{-\frac{j2Ksin(\theta)}{R_L}} = \frac{1}{2}R_L(1 + j * cot(\theta)) \quad (2.7)$$

$$Z_1{}' = \frac{V_1}{I_1} \quad (2.8)$$

$$I_1 = j * I_{Load}\frac{Z_0}{R_L} = 2Kcos(\theta)\frac{{Z_0}^2}{R_L}$$

$$Z_1{}' = \frac{Ke^{j\theta}}{2Kcos(\theta)\frac{{Z_0}^2}{R_L}} = \frac{1}{2}\frac{{Z_0}^2}{R_L}[1 + jtan(\theta)] \quad (2.8)$$

$$Z_2{}' = \frac{V_2}{I_2} \quad (2.9)$$

$$I_2 = j * I_{Load}\frac{Z_0}{R_L} = 2Kcos(\theta)\frac{{Z_0}^2}{R_L}$$

$$Z_2{}' = \frac{V_2}{I_2} = \frac{1}{2}\frac{{Z_0}^2}{R_L}[1 - jtan(\theta)] \quad (2.9)$$

$$I_{Load} = \frac{-jV_1}{Z_0} + \frac{-jV_2}{Z_0} = \frac{-j2Kcos(\theta)}{Z_0} \quad (2.10)$$

$$I_{Load} = (I_1 + I_2) = 2Kcos(\theta) \quad (2.11)$$

$$Z_1 = \frac{V_1}{I_1} = \frac{2Kcos(\theta)}{Ke^{j\theta}} R_L = 2 * R_L \left(cos(\theta)^2 - j\frac{sin(2\theta)}{2}\right) \quad (2.12)$$

$$Z_2 = \frac{V_2}{I_2} = \frac{2Kcos(\theta)}{Ke^{-j\theta}} R_L = 2 * R_L \left(cos(\theta)^2 + j\frac{sin(2\theta)}{2}\right) \quad (2.13)$$

Eq. 2.17

Class B efficiency

$$\eta = \frac{P_{out}}{P_{DC}}$$

$$P_{out} = \left(\frac{V_{out}}{\sqrt{2}}\right)^2 \frac{1}{R_L}$$

$$P_{DC} = V_{DC} * I_{DC}$$

$$I_{DC} = \frac{1}{2\pi}\int_0^{\pi} I_{max} * \sin(\theta)\, d\theta + \int_{\pi}^{2\pi} 0 = -\frac{1}{2\pi} Imax[\cos(\pi) - \cos(0)] = \frac{1}{\pi} I_{max}$$

$$I_{max} = \frac{2V_{out}}{R_L}$$

$$I_{DC} = \frac{1}{\pi}\frac{2V_{out}}{R_L}$$

Efficiency of each PA operating with the Chireix Combiner

$$V_{out} = I_L * R_L = 2Kcos(\theta)R_L$$

$V_{DC} = 2 * K * R_L$, K is the amplitude of the current source and V_{DC} is the maximum of the value that V_{out} can assume.

$$\eta = \frac{Vout^2}{2*R_L} * \frac{\pi * R_L}{2V_{out}*V_{DC}} = \frac{\pi}{4}\frac{V_{out}}{V_{DC}} = \frac{\pi}{4}\cos(\theta) \quad (2.16)$$

$$Y_1 = \frac{I_1}{V_1} \tag{2.18}$$

$$I_1 = \frac{jV_{out}}{Z_0} * R_L = \frac{2Kcos(\theta)R_L}{Z_0^2}$$

$$Y_1 = \frac{2Kcos(\theta)R_L}{Z_0^2 * Ke^{j\theta}} = \frac{2*R_L}{{Z_0}^2}\left(cos(\theta)^2 - j\frac{sin(2\theta)}{2}\right) \tag{2.18}$$

$$Y_2 = \frac{I_2}{V_2} \tag{2.19}$$

$$I_2 = \frac{jV_{out}}{Z_0} * R_L = \frac{2Kcos(\theta)R_L}{Z_0^2}$$

$$Y_2 = \frac{2Kcos(\theta)R_L}{Z_0^2 * Ke^{-j\theta}} = \frac{2*R_L}{{Z_0}^2}\left(cos(\theta)^2 + j\frac{sin(2\theta)}{2}\right) \tag{2.19}$$

Determining the Fourier coefficients of a function representing a step

$$a_n = \frac{2}{T}\int_{-\pi}^{\pi} f(x) * \cos\left(\frac{2\pi nx}{T}\right) dx \tag{3.2}$$

$$b_n = \sum_{n=0}^{\infty} \frac{2}{T} \int_{-\pi}^{\pi} f(x) * \sin\left(\frac{2\pi kx}{T}\right) dx \tag{3.3}$$

$$a_0 = \frac{2}{2\pi}\int_{-\pi}^{\pi} f(x)\cos(nx)dx = \frac{1}{\pi}\int_0^{\pi} \cos(o)\, dx = 1$$
$$a_1 = \frac{2}{2\pi}\int_{-\pi}^{\pi} f(x)\cos(nx)dx = \frac{1}{\pi}\int_0^{\pi} \cos(x)\, dx = 0$$
$$a_n = \frac{2}{2\pi}\int_{-\pi}^{\pi} f(x)\cos(nx)dx = \frac{1}{\pi}\int_0^{\pi} \cos(nx)\, dx = 0$$
$$b_0 = \frac{2}{2\pi}\int_{-\pi}^{\pi} f(x)\sin(nx)dx = \frac{1}{\pi}\int_0^{\pi} \sin(0)\, dx = 0$$
$$b_1 = \frac{2}{2\pi}\int_{-\pi}^{\pi} f(x)\sin(nx)dx = \frac{1}{\pi}\int_0^{\pi} \sin(x)\, dx = \frac{2}{\pi}$$
$$b_2 = \frac{2}{2\pi}\int_{-\pi}^{\pi} f(x)\sin(nx)dx = \frac{1}{\pi}\int_0^{\pi} \sin(2x)\, dx = 0$$
$$b_3 = \frac{2}{2\pi}\int_{-\pi}^{\pi} f(x)\sin(nx)dx = \frac{1}{\pi}\int_0^{\pi} \sin(3x)\, dx = -\frac{2}{3\pi}$$

Appendix C

(Matlab code)

Outphasing concept

```
%% Author: João Lucas, 60188
% Chireix Amplifier

% This script pretends to simulate a reconstruction of a signal
% modulated in amplitude, using outphasing method.

%% Firstly, the input signal is modulated in phase, yielding 2 PM
signals,
% then these signals are summed, to reconstruct the original
signal, modulated in amplitude.

%%

 f = 1*10^6; % operation frequency

range = 2*2 % maximum amplitude at output
A = 1; %amplitude required

maxA = range/2;



w = 2*pi*f; % angular frequency
t = 0:1*10^-10:10^-6;

Sin = A.*cos(w.*t); % input wave
figure
plot(t,Sin); %

% designing 2 circles
%%%%%%%%%%%%%%%%%%%
figure
x = 0; y = 0; r = maxA;
ang = 0:0.01:2*pi;
xp = r*cos(ang);
yp = r*sin(ang);
plot(x+xp,y+yp,'g');
hold on;
r = 2*maxA;
xp = r*cos(ang);
yp = r*sin(ang);
```

```
plot(x+xp,y+yp);
hold on;
N = length(Sin-1);
%designing amplitude vector of input wave
if(Sin(N) >= 0)
    plot(0:0.1*A:A,0,'r');
end
if(Sin(N) < 0)
    plot(A:0.1*A:0,0,'r');
end

%calculating "fi"
% cos(A) + cos(B) = 2cos(fi)cos(wt) => A = wt + fi and B = wt - fi
% in the previous eq, A and B are angles
% Acos(wt)-> input wave, in this equation A is the wave amplitude
% 2cos(fi)cos(wt) = Acos(wt)
% <=> fi = acos(A/2)
fi = acos(A/maxA/2);
acosd(A/maxA/2) %degrees
S1 = maxA*cos(w.*t+fi);
S2 = maxA*cos(w.*t-fi);

hold on;
% calculating amplitude vectors of sinal 1 and 2
vector1 = maxA*exp(j*fi);
vector2 = maxA*exp(-j*fi);
% designing vectores in image of circles
plot(real(vector1),imag(vector1),'o');
plot(real(vector2),imag(vector2),'x');
legend('amplitude of each amplifier', 'maximum amplitude at the
output');

% vectors sum -> have to be equal to original signal amplitude
abs(vector1+vector2)

% designing all signals
figure
Sout = S1 + S2;
plot(t,Sin,'g.',t,S1,'r',t,S2,'b',t,Sout,'k--');
legend('input wave', 'phased wave - 1', 'phased wave - 2', 'output
wave');

%%
%Bibliography:
    % RF POWER AMPLIFIERS FOR WIRELESS COMMUNICATIONS, STEVE C.
CRIPPS
```

Signals generated to measure the PA Outphasing/Chireix

Script used to do AM/Outphasing modulation

```
function [Pin,PHASE_DIFF] = Chireix_powerSplit(Pinput,Pmax)

echo on;

% Output variables
% Pin -> power to send to each PA
% PHASE_DIFF -> phase difference between each signal

% Input variables
% Pinput -> virtual power generated -> range[0;70]
% Pmax -> maximum power to provide at each PA -> range[25;27]
if(Pmax < 25 || Pmax > 27)
    Pmax = 26;
    sprintf('Pmax is not well defined and was set to 26, please
chose a value between 25 and 27')
end

if (Pinput <= Pmax)
    Pin = Pinput;
    PHASE_DIFF = 2*(acos(Pmax/70))*360/(2*pi);
else
    if ( Pinput > Pmax && Pinput <= 70)
        PHASE_DIFF = 2*radtodeg(acos(Pinput/70));
        Pin = Pmax;
    else
        Pinput = 70;
        PHASE_DIFF = 2*radtodeg(acos(Pinput/70));
        Pin = Pmax;
        sprintf('Pinput greater than the maximum value allowed,
range [0;70]')
    end
end

echo off

end
```

Script used to linearize the system (mix mode)

```
function [Pavs, PHASE] = Chireix_linear(Pinput,PMax,PinputMax)

% Input variables
% Pinput is the input power of the system range[PMin;(PinputMax-
0.5)]
% Pinput = PMin:0.5:(PinputMax-0.5); -> PinputMax = 28
%   PinputMax defines the final gain, final_Gain = (Pout_dbm -
PinputMax)
% PMax defines the maximum power to provide at both PAs; PMax =
29;

% Output variables
% Pavs -> Power to provide to each PA
% PHASE -> phase difference between each PA and with negative sign
to
    % provide at second PA (lower PA) (lower)


PMin = -20; %% smallest signal to be aplied at the sytem
%PMax = 29; %% sum of the power provided at each PA

%syms x;
%y = -3+(PMax)*sin(((x)/(PMax))*(pi/2))^2;
%dy = diff(y);
%m = 1;
%a = solve('pi*cos((pi*x)/52)*sin((pi*x)/52) = 1');
%a = double(a(2));
%yx = -3+(PMax)*sin(((a)/(PMax))*(pi/2))^2;
%b = yx-m*a;
%PMin_phase = PMax - (PMax/pi)*asin(2/pi);
PMin_phase = PMax - (PMax/pi)*asin(2/pi);
%PinputMax = 28;
initPhase = 95;
expoente = 0.5;
PMax = 29;
%Pinput = PMin:0.5:(PinputMax-0.5);
%errorGain = ((PMax)*sin((round(PMin_phase)/(PMax))*(pi/2))-
round(PMin_phase));
errorGain =
((PMax)*sin(((round(PMin_phase*100)/100)/(PMax))*(pi/2))^2-
(round(PMin_phase*100)/100))
%errorGain = ((PMax)*sin((PMin_phase/(PMax))*(pi/2))^2-
PMin_phase);


if (PMax < 25)
    PMax = 25;
    display('Pmax exceed the minimum range -> 25 was set to
Pmax');
end
```

```
if (PMax > 30)
    PMax = 30;
    display('Pmax exceed the maximum range -> 30 was set to
Pmax');
end


if ((Pinput) > 31)
    Pinput = 31;
    display('Pinput exceed the maximum range -> 31 was set to
Pinput');
end


if ((Pinput) > 0)
        PHASE =
cos((Pinput)/((PinputMax)/(pi/2)))^expoente*initPhase;
    else
        PHASE = initPhase;
end

if( Pinput > (round(PMin_phase*100)/100)  && Pinput <= PMax)
        Pavs = -3+(PMax)*sin(((Pinput)/(PMax))*(pi/2))^2 ;
elseif  ((Pinput) > PMax)
    Pavs = -3+PMax;
else
    Pavs = -3+(Pinput) + errorGain ;
end

end
```